
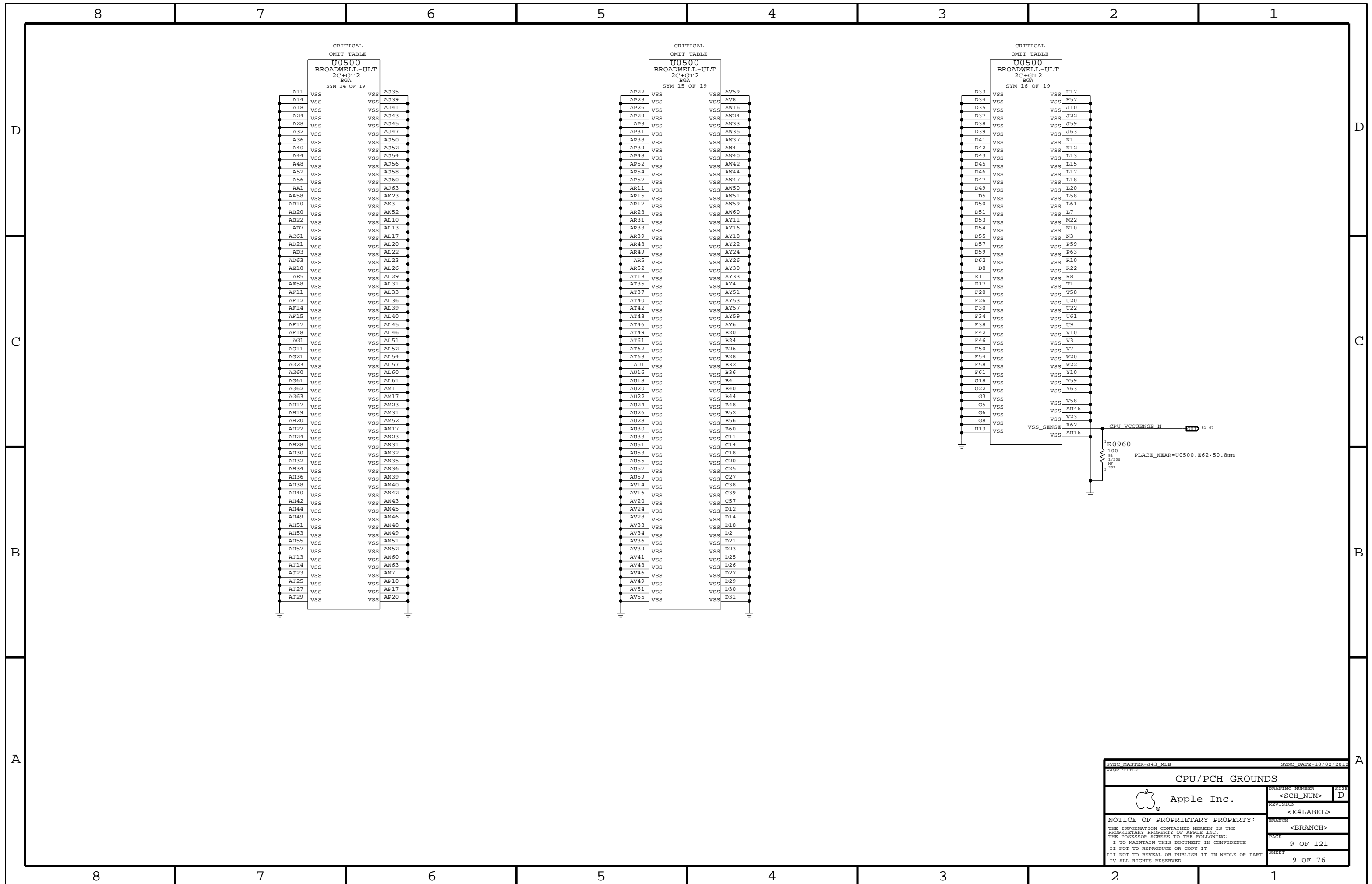
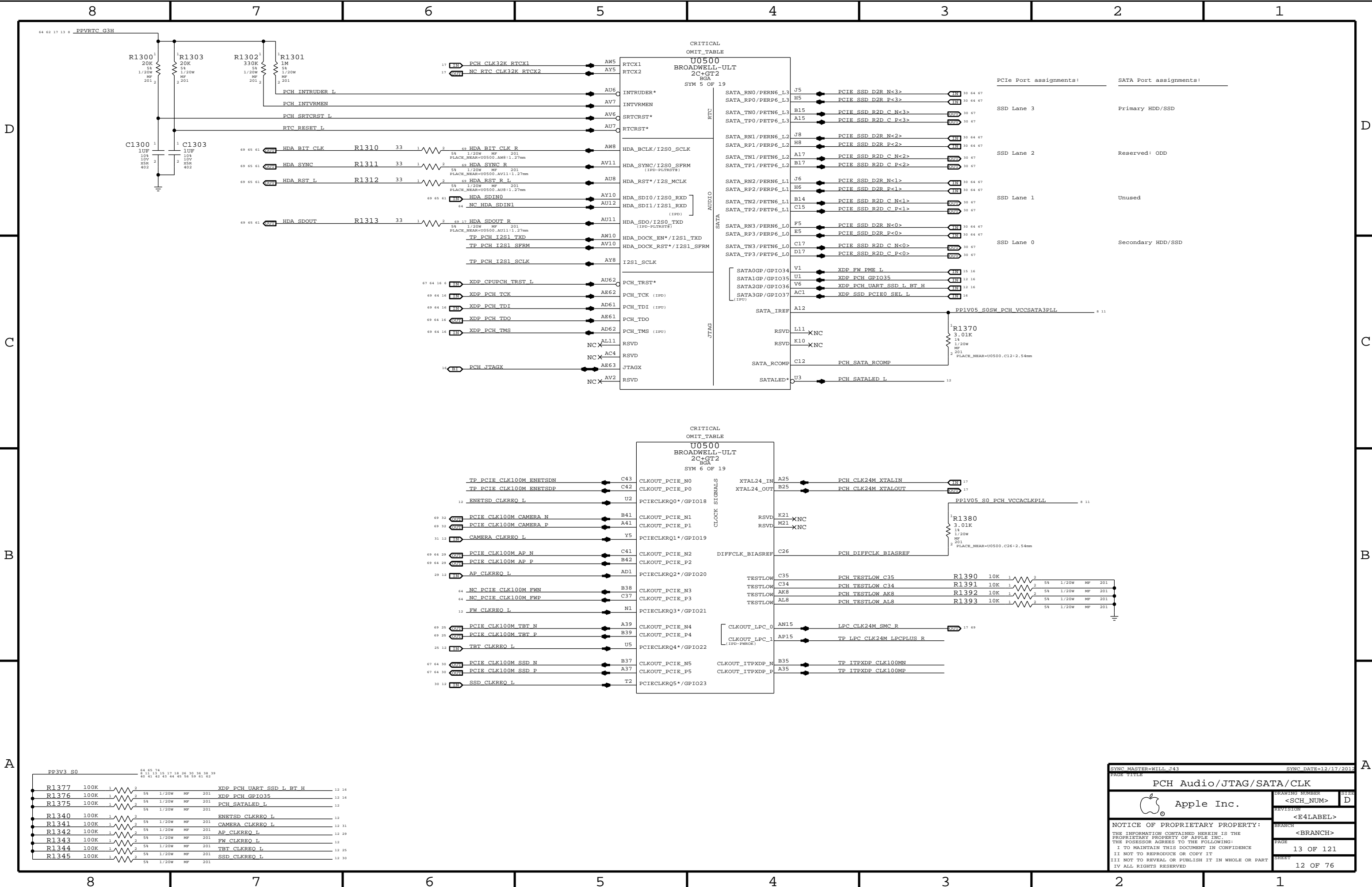


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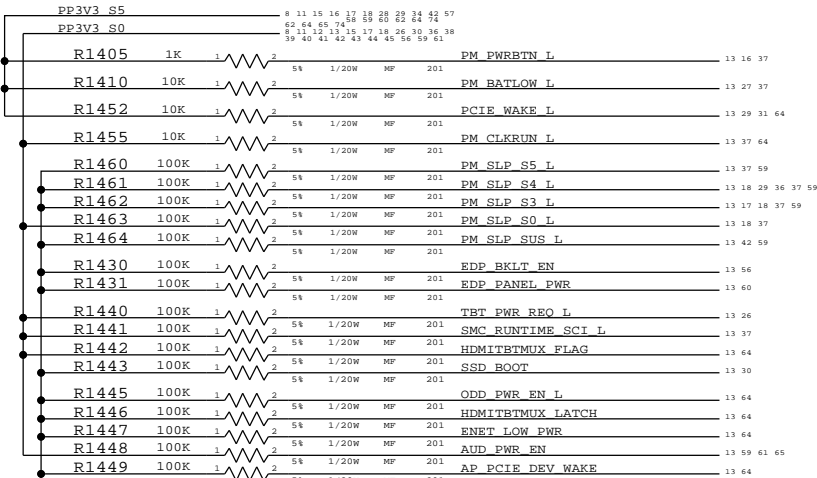
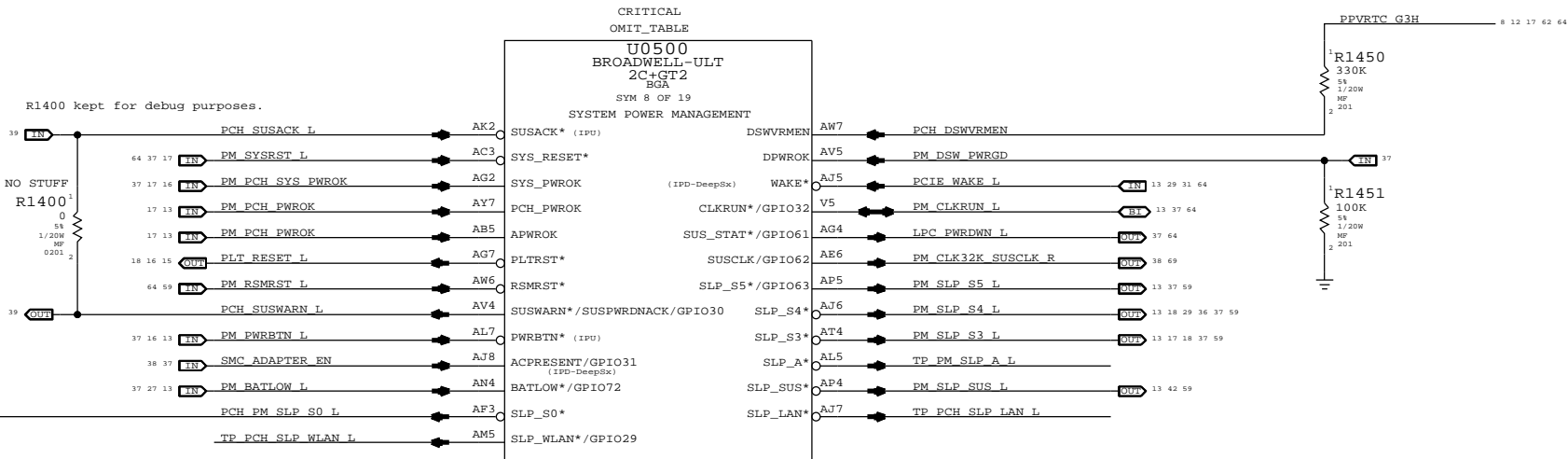
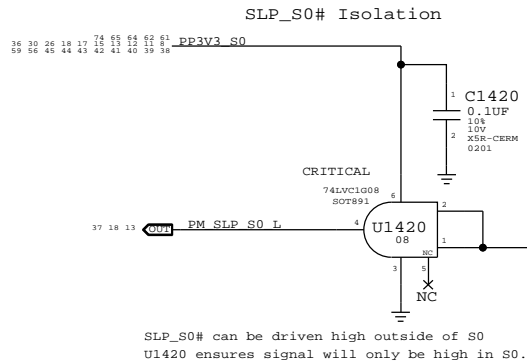
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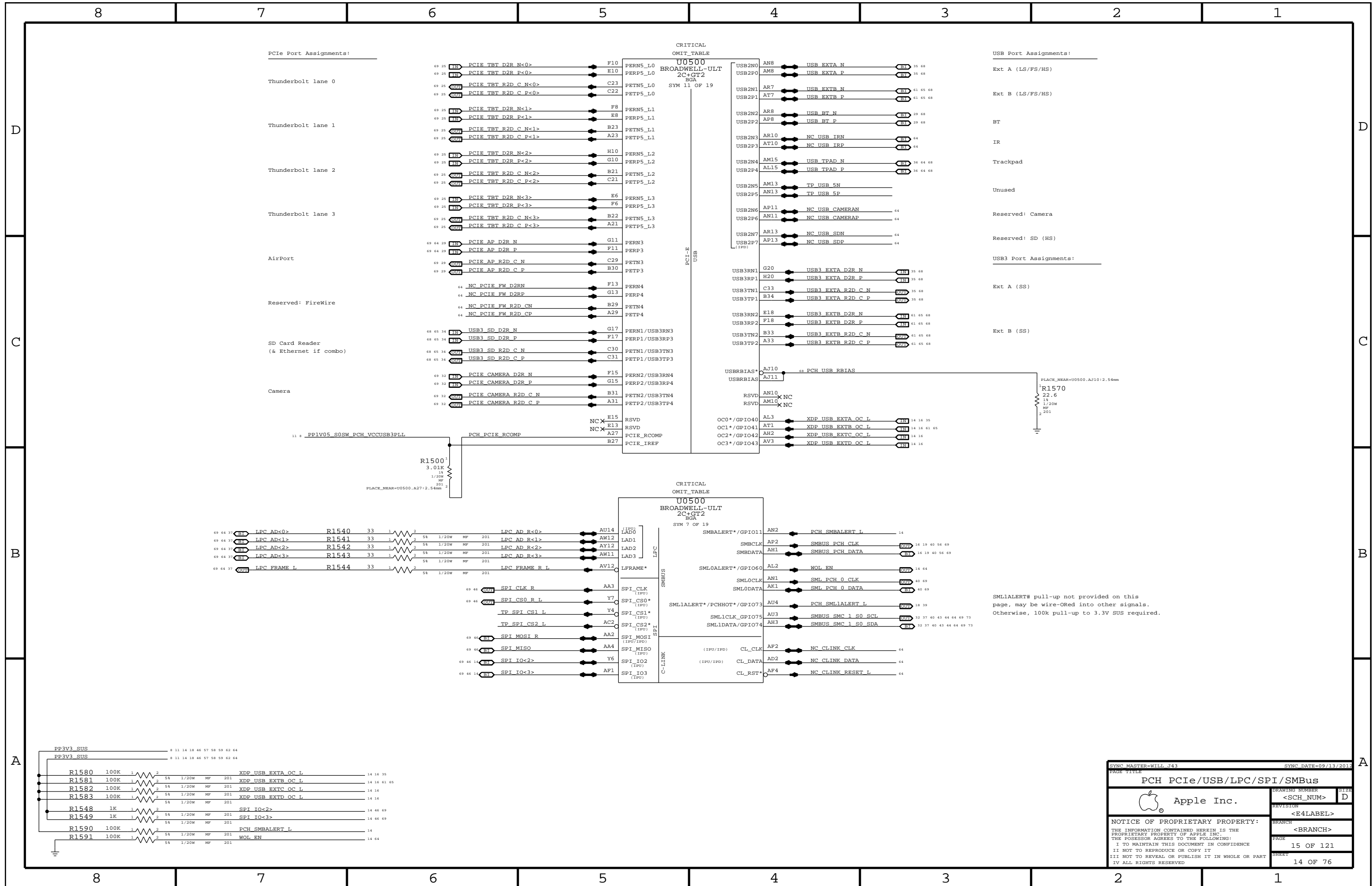
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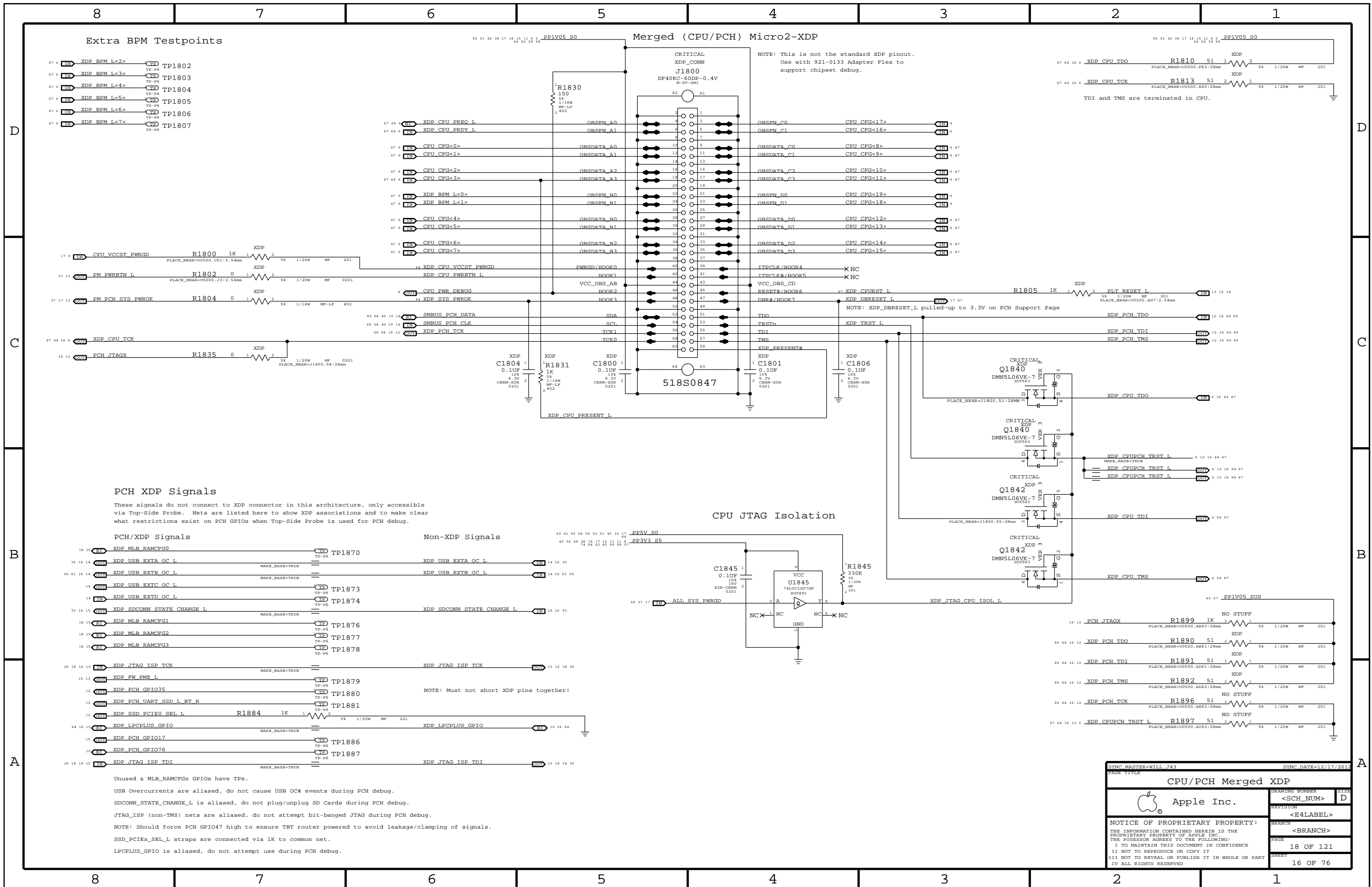
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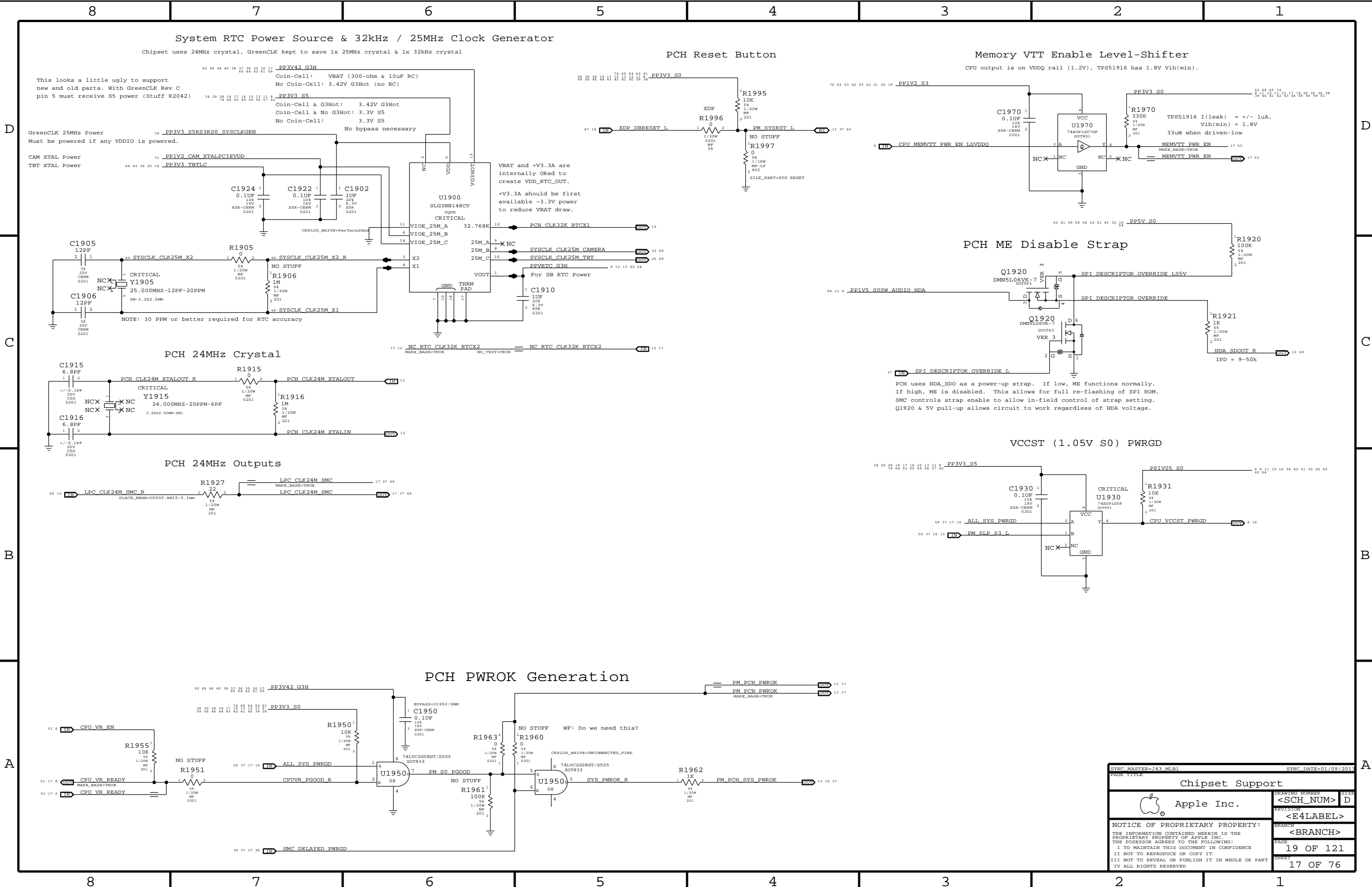


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System RTC Power Source & 32kHz / 25MHz Clock Generator

Chipset uses 24MHz crystal, GreenCLK kept to save 1x 25MHz crystal & 1x 32kHz crystal

This looks a little ugly to support new and old parts. With GreenCLK Rev C pin 5 must receive S5 power (Stuff R2042)

GreenCLK 25MHz Power
Must be powered if any VDDIO is powered.

CAM XTAL Power

TBT XTAL Power

PCH Reset Button

Memory VTT Enable Level-Shifter


CPU output is on VDDQ rail (1.2V), TPS51916 has 1.8V Vih(min).

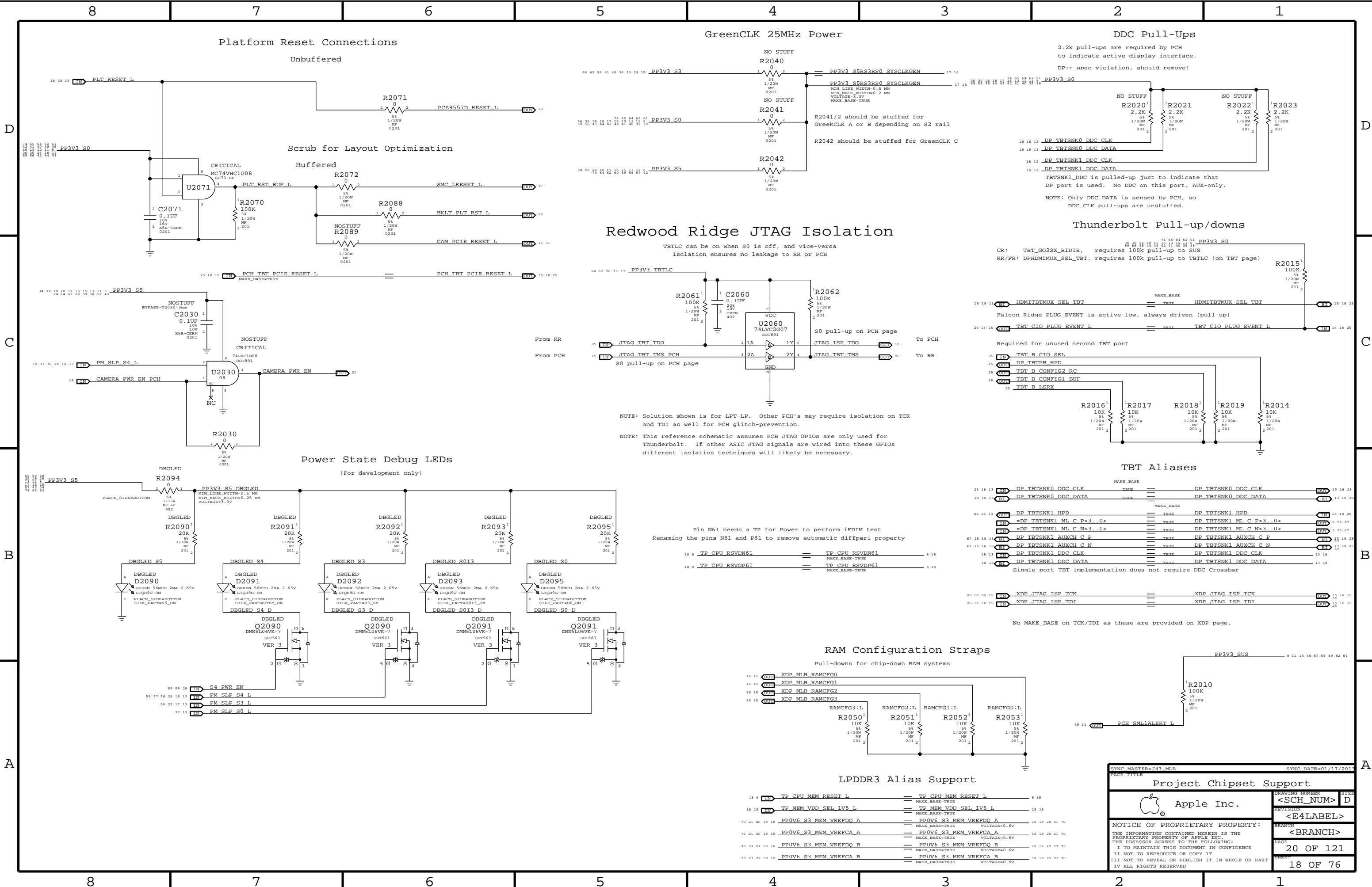
PCH ME Disable Strap

PCH uses HDA_SDO as a power-up strap. If low, ME functions normally. If high, ME is disabled. This allows for full re-flashing of SPI ROM. SMC controls strap enable to allow in-field control of strap setting. Q1920 & 5V pull-up allows circuit to work regardless of HDA voltage.

VCCST (1.05V S0) PWRGD

PCH PWROK Generation

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Chipset Support			
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Power aliases required by this page:

- =PP3V3_S3_VREFMRGN
- =PPDDR_S3_MEMVREF

Signal aliases required by this page:

- =I2C_VREFDAC5_SCL
- =I2C_VREFDAC5_SDA
- =I2C_PCA9557D_SCL
- =I2C_PCA9557D_SDA

BOM options provided by this page:

- DDRVREF_DAC - Stuffs DAC margining circuit.

FETs for CPU isolation during DAC margining

NOTE: CPU DAC output step sizes:

DDR3	(1.5V)	7.70mV per step
DDR3L	(1.35V)	6.99mV per step
LPDDR3	(1.2V)	??.?mV per step

NOTE: CPU has single output for VREFCA. Split into two signals for independent DAC margining support. When DAC margining VREFCA ensure VREFMRGN_CPU_EN is low to remove short due to CPU.

DAC sets voltage level, PCA9557 & FETs enable outputs and disables margining after platform reset.

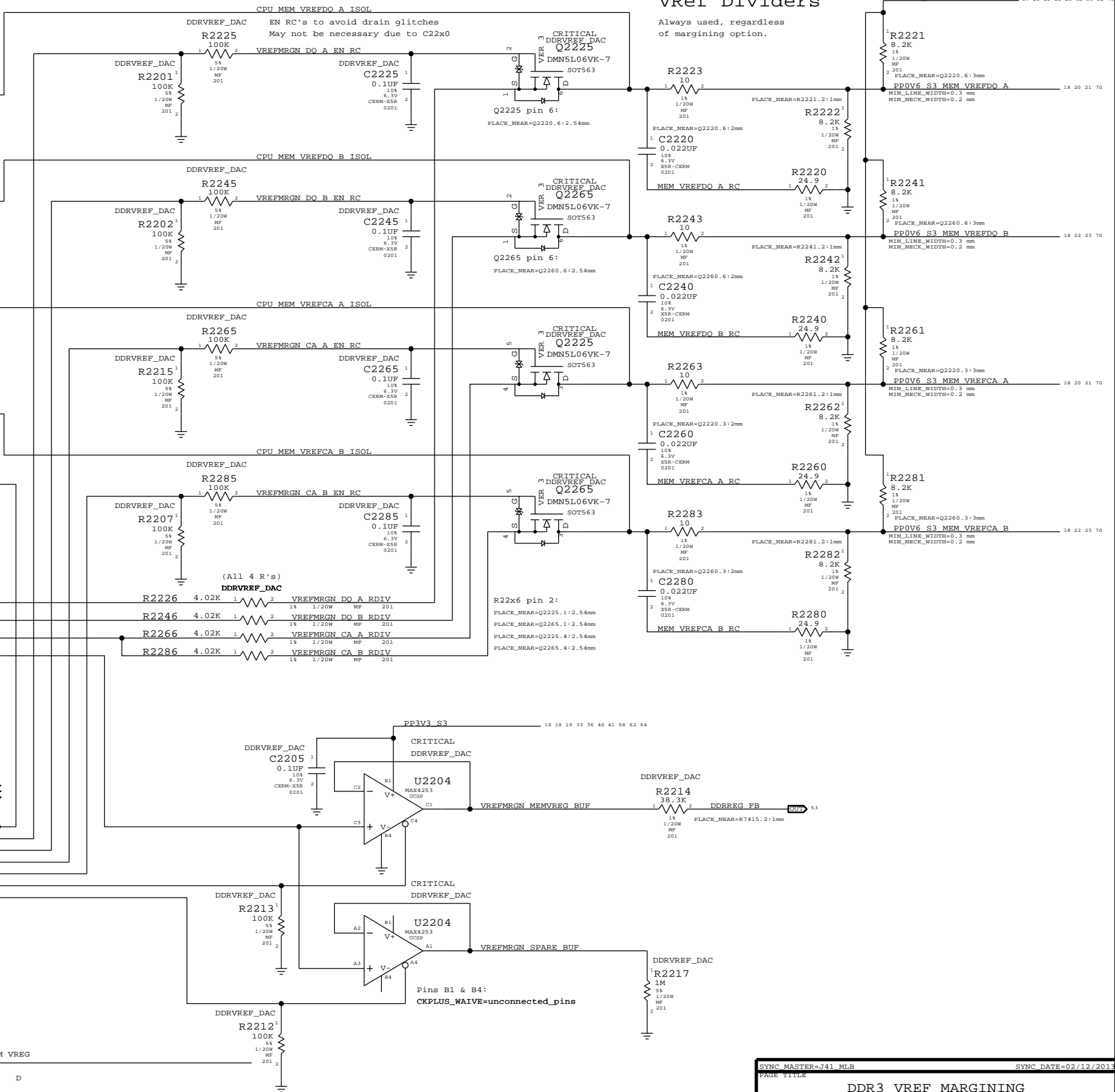
RST* on 'platform reset' so that system watchdog will disable margining.


NOTE: Margining will be disabled across all soft-resets and sleep/wake cycles.

	MEM A VREF DQ	MEM B VREF DQ	MEM A VREF CA	MEM B VREF CA	MEM VREG
DAC Channel:	A	B	C	C	D
PCA9557D Pin:	1	2	3	4	5
	LPDDR3 (1.2V)		DDR3L (1.35V)		LPDDR3 (1.2V) DDR3L (1.35V)
Nominal value	0.600V (DAC: 0x2E.5)		0.675V (DAC: 0x34)		1.200V (DAC: 0x5D) 1.343V (DAC: 0x68)
Margined target:	0.300V - 0.900V (+/- 300mV)		0.337V - 1.013V (+/- 337.5mV)		0.800V - 1.600V (+/- 400mV) 0.972V - 1.714V (+/- 371mV)
DAC range:	0.000V - 1.199V (0x00 - 0x5D)		0.000V - 1.354V (0x00 - 0x69)		0.000V - 2.397V (0x00 - 0xBA) 0.000V - 2.694V (0x00 - 0xD1)
VREF current:	+73uA - -73uA (- = sourced)		+82uA - -82uA (- = sourced)		+21uA - -21uA (- = sourced) +25uA - -25uA (- = sourced)
DAC step size:	6.36mV / step @ output		6.36mV / step @ output		4.28mV / step @ output 3.53mV / step @ output

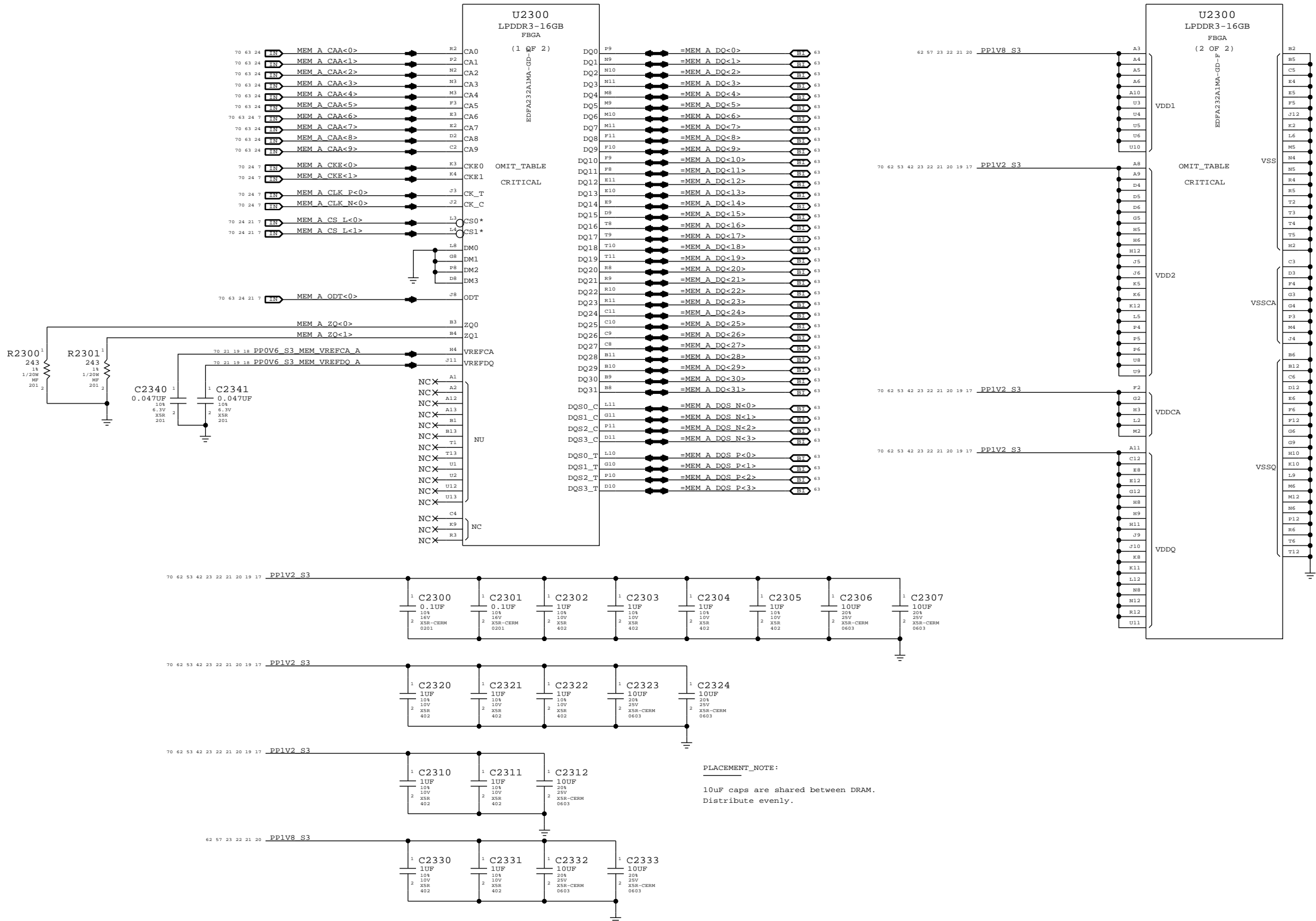
NOTE: LPDDR3 assumes TPS51916 supply with 28.7k/57.6k divider
DDR3L assumes TPS51916 supply with 19.6k/57.6k divider

Always used, regardless
of margining option.

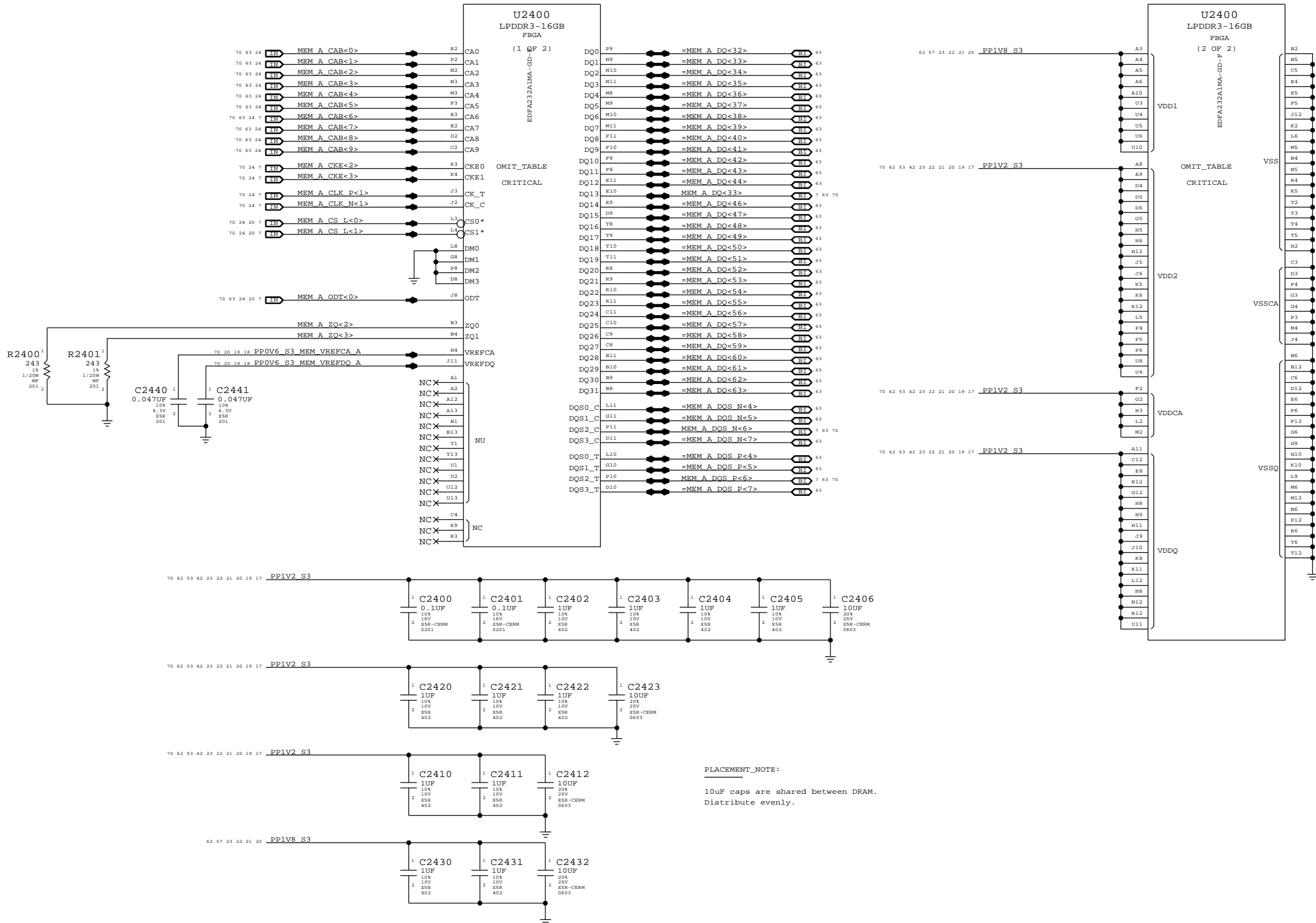


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LPDDR3 CHANNEL A (0-31)



LPDDR3 CHANNEL A (32-63)



PLACEMENT_NOTE:
10uF caps are shared between DRAM.
Distribute evenly.

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LPDDR3 DRAM Channel A (32-63)			
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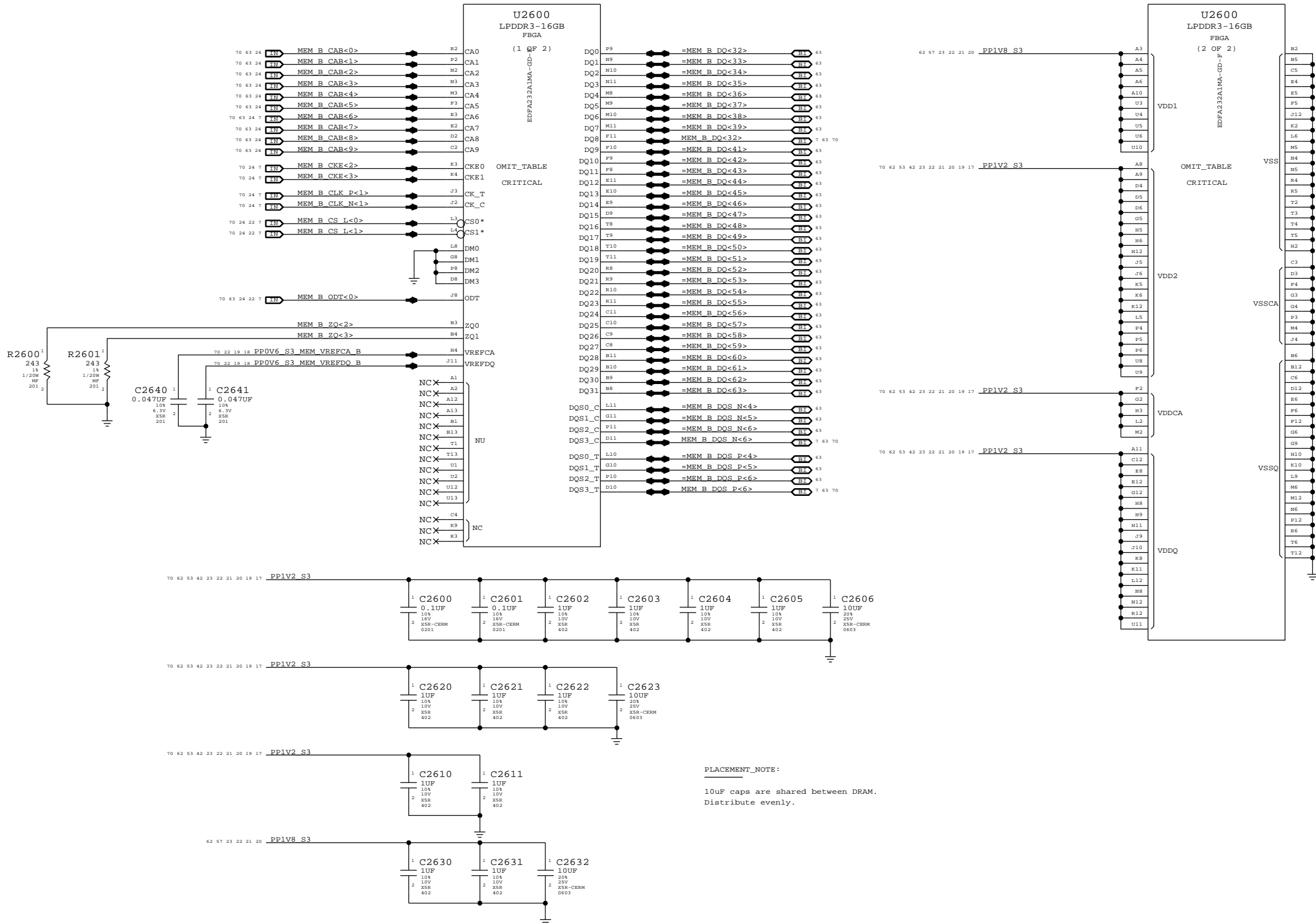
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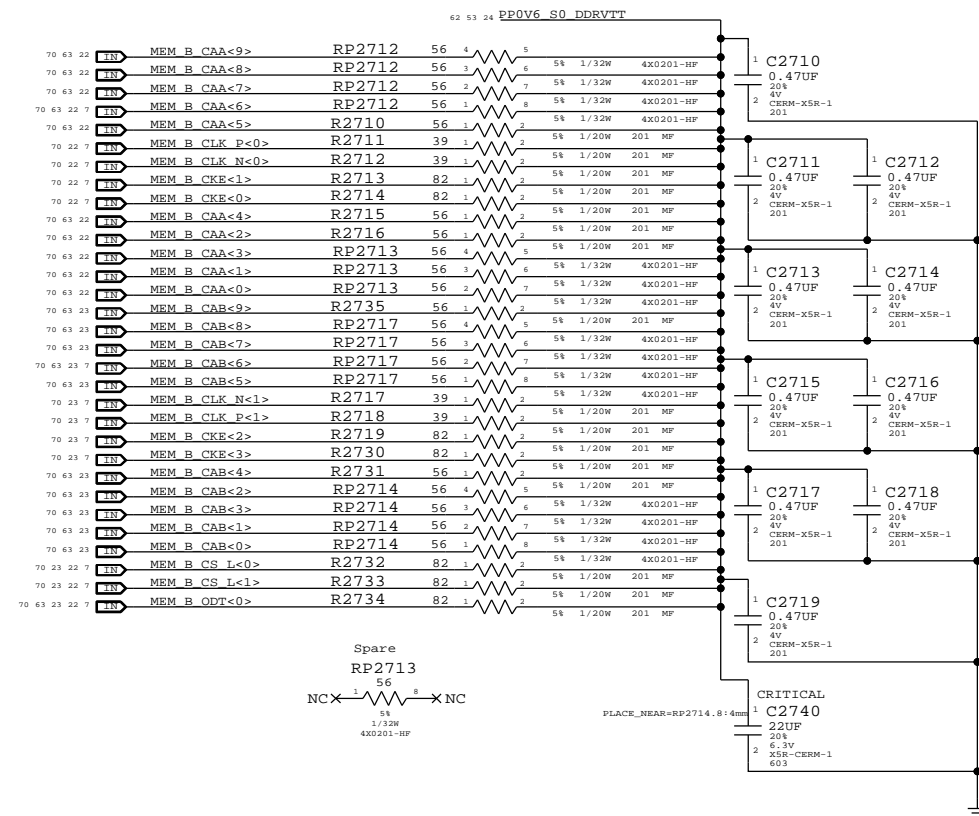
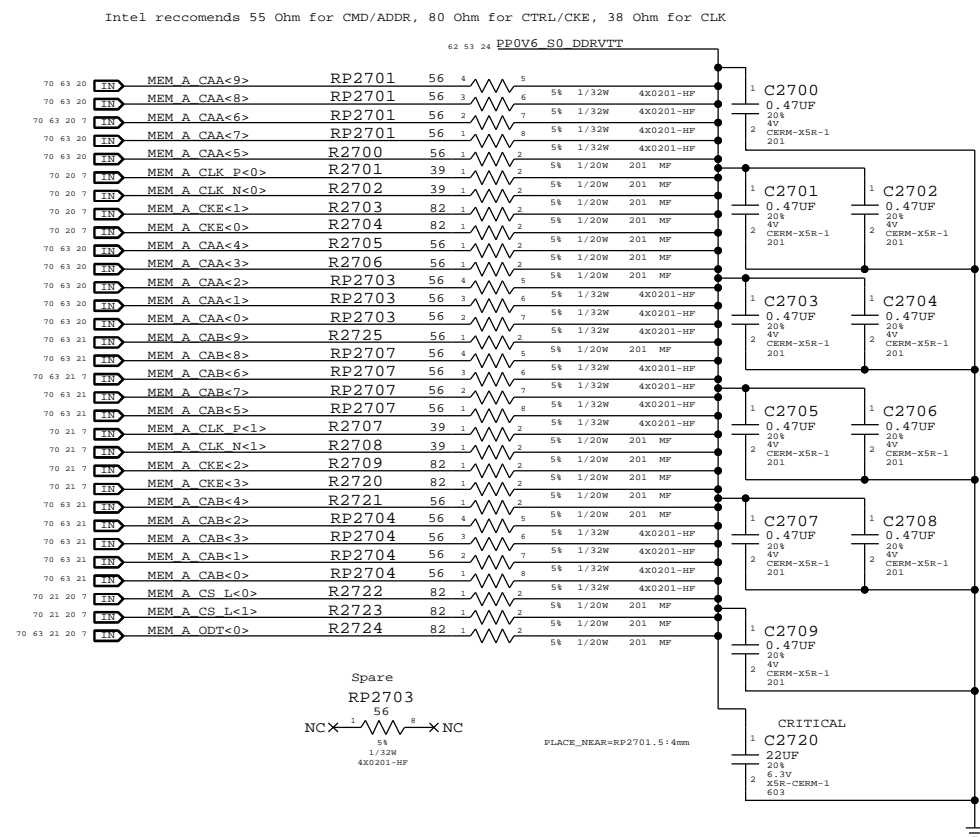


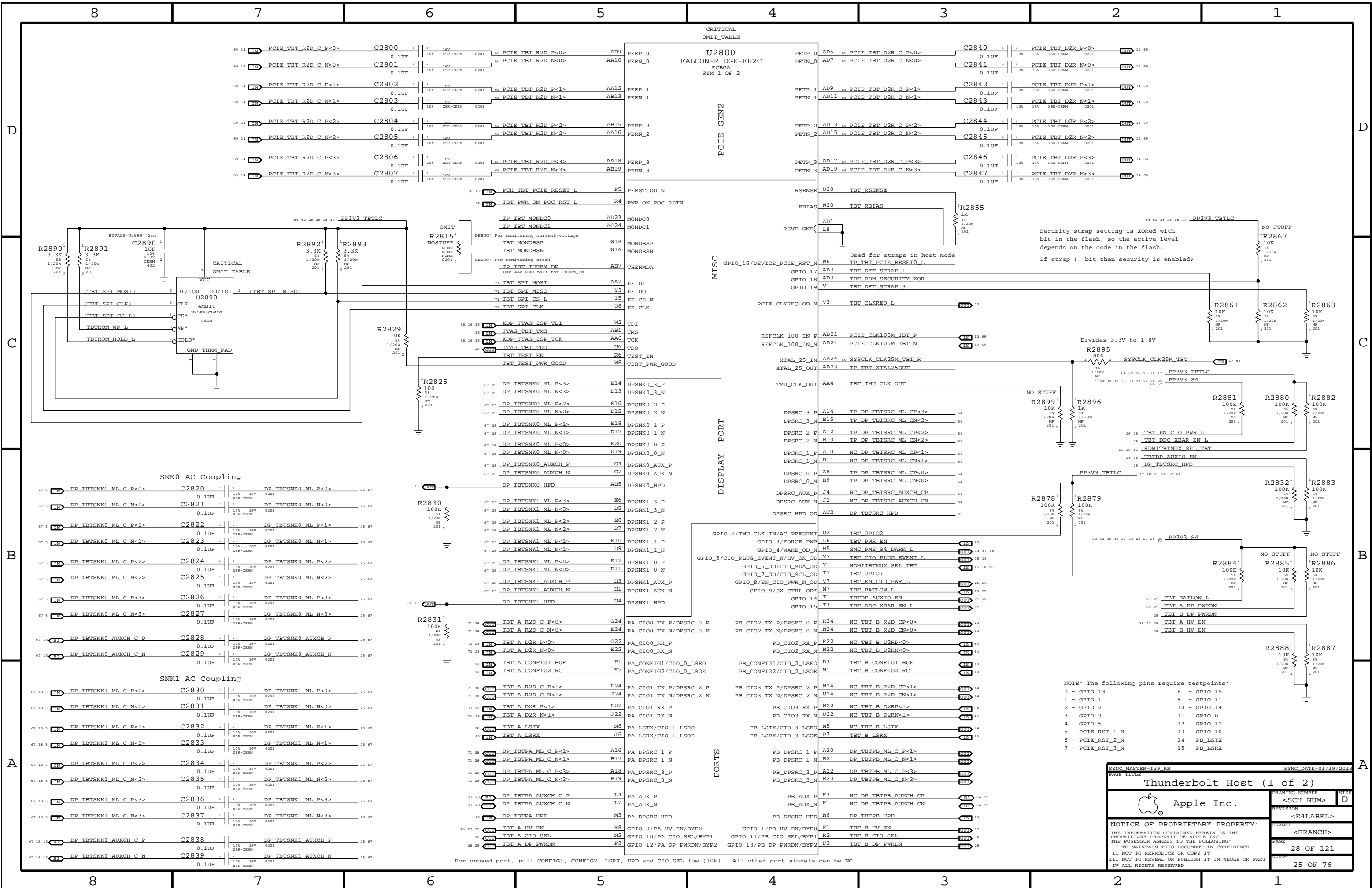
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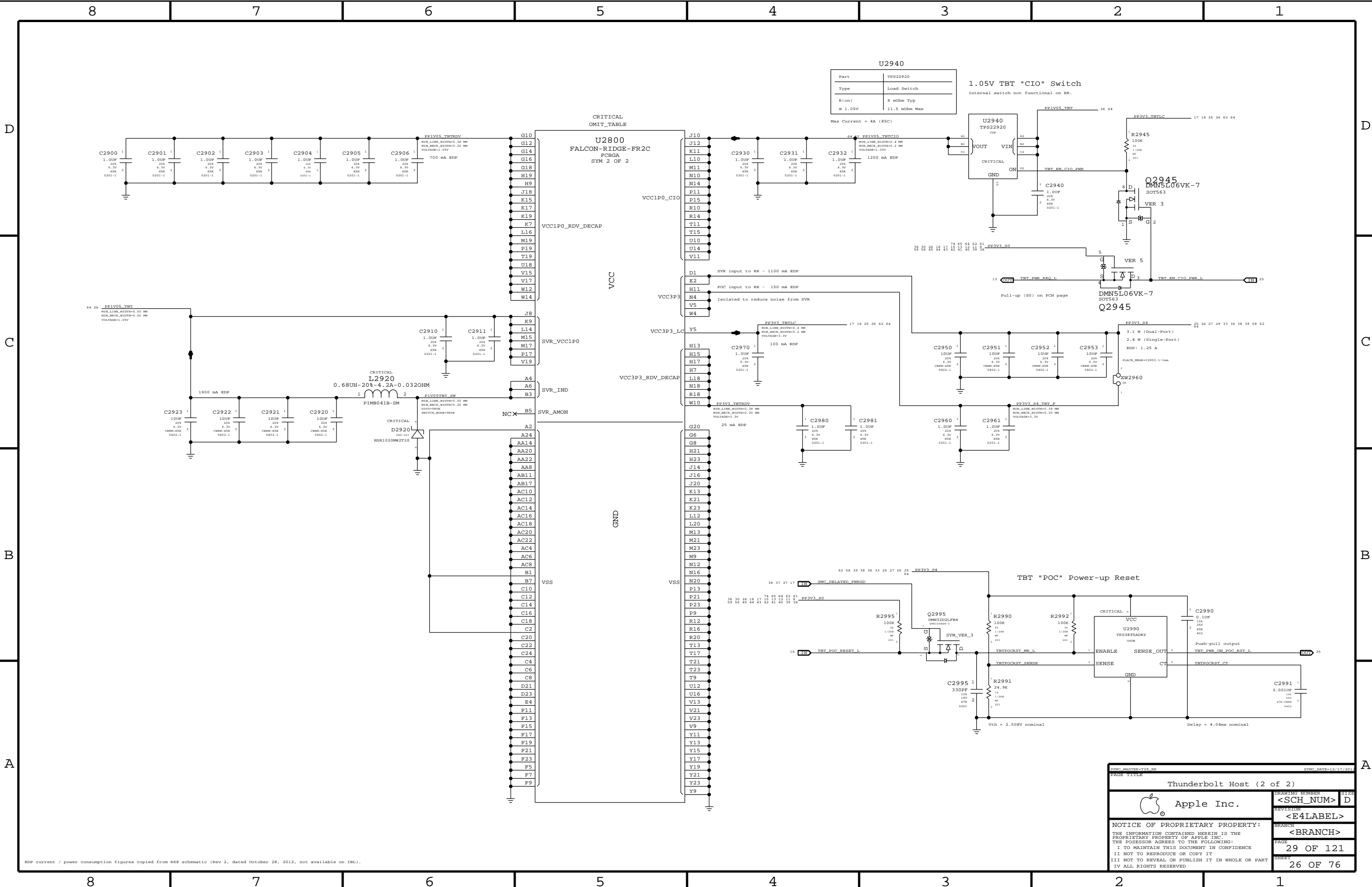
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LPDDR3 CHANNEL B (32-63)









Part	TPS22920
Type	Load Switch
R(on)	8 mOhm Typ @ 1.05V 11.5 mOhm Max

1.05V TBT "CIO" Switch
Internal switch not functional on RR.

Max Current = 4A (85C)


CRITICAL
OMIT_TABLE
U2800
FALCON-RIDGE-FR2C
FCBGA
SYM 2 OF 2

VCC

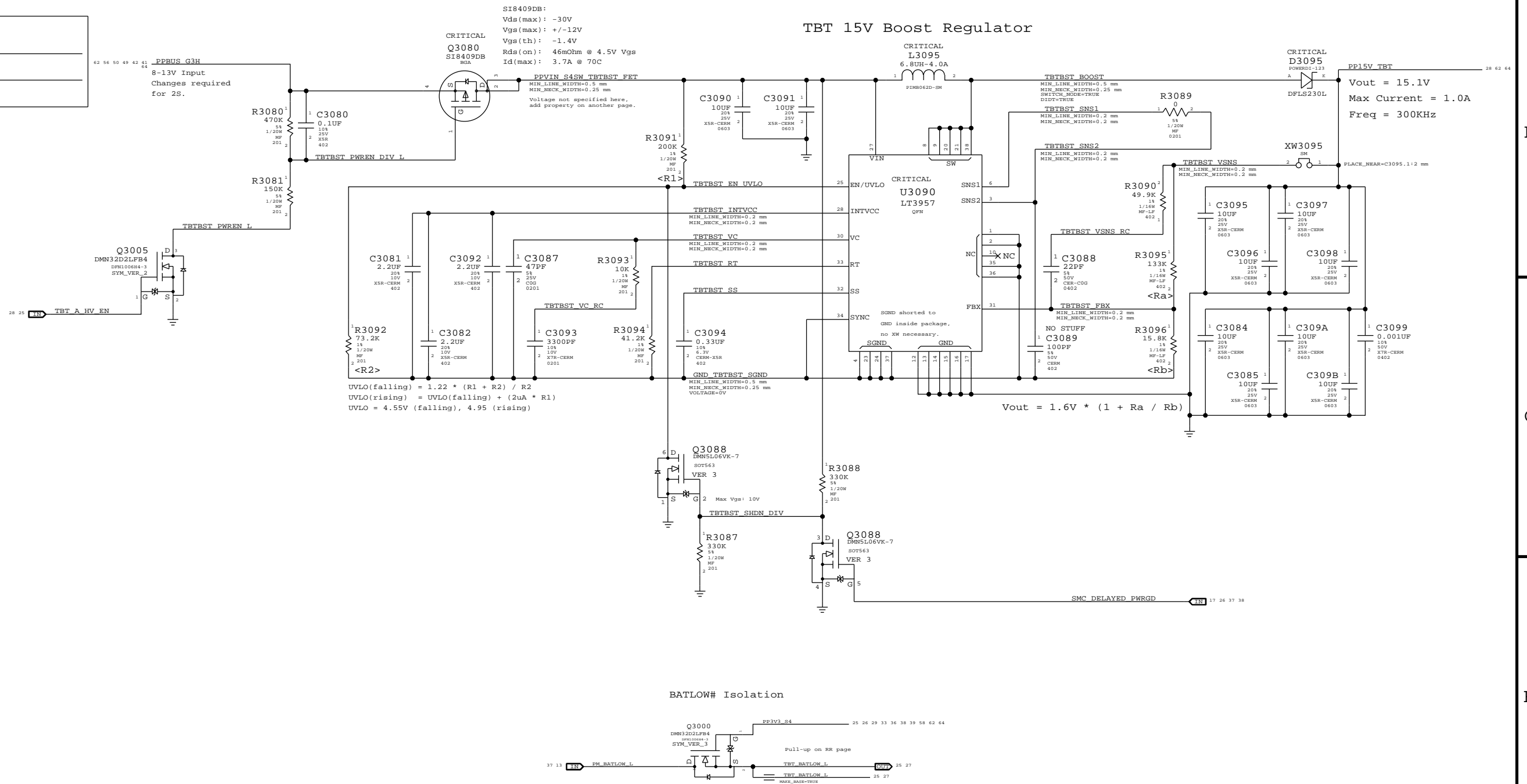
GND


VSS

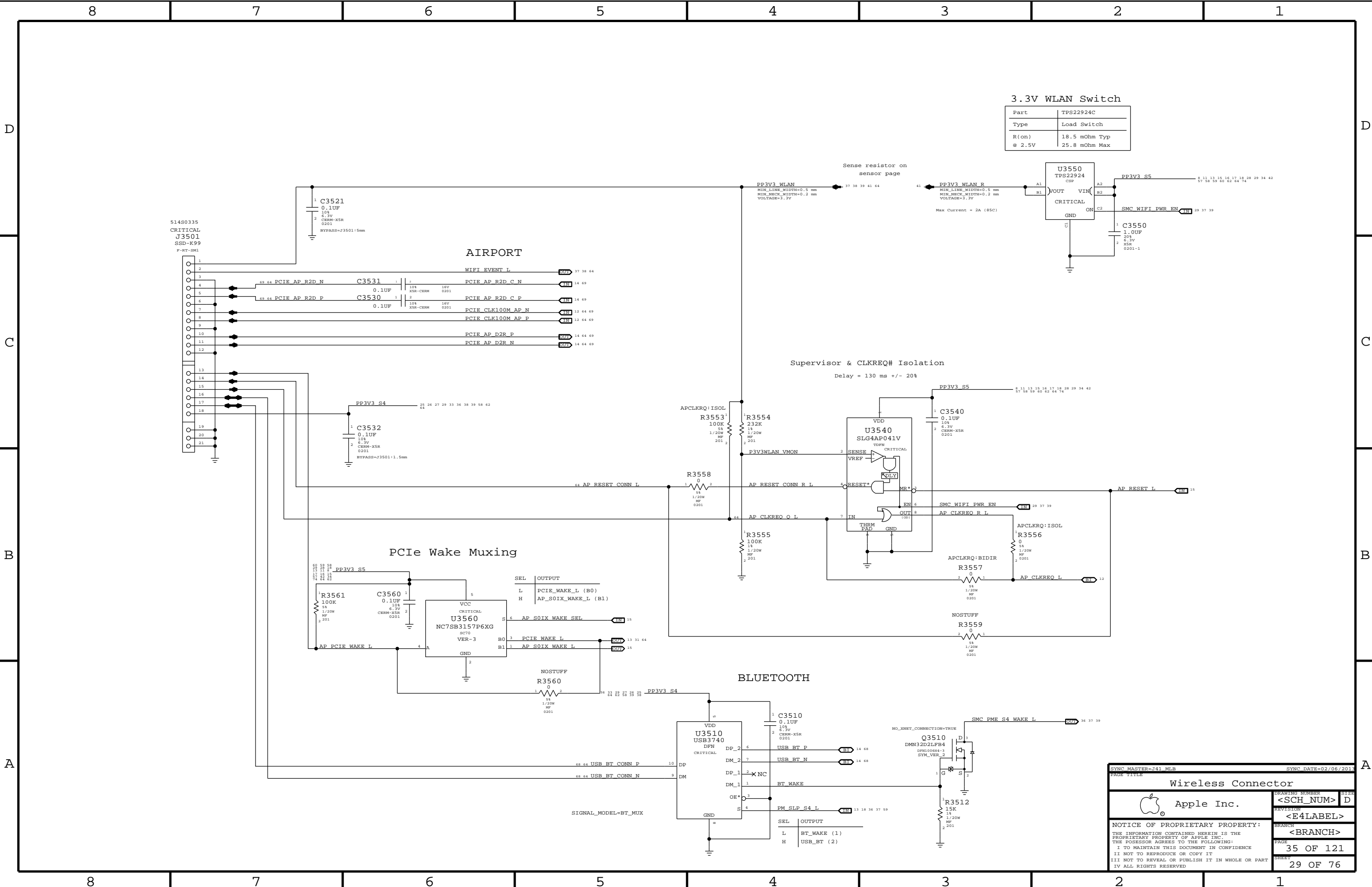
TBT "POC" Power-up Reset

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EDP current / power consumption figures copied from R68 schematic (Rev 2, dated October 28, 2012, not available on IBL).



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3.3V WLAN Switch


Part	TPS22924C
Type	Load Switch
R(on) @ 2.5V	18.5 mOhm Typ 25.8 mOhm Max

SYNC MASTER=J41 MLB

SYNC DATE=02/06/2013

PAGE TITLE

Wireless Connector

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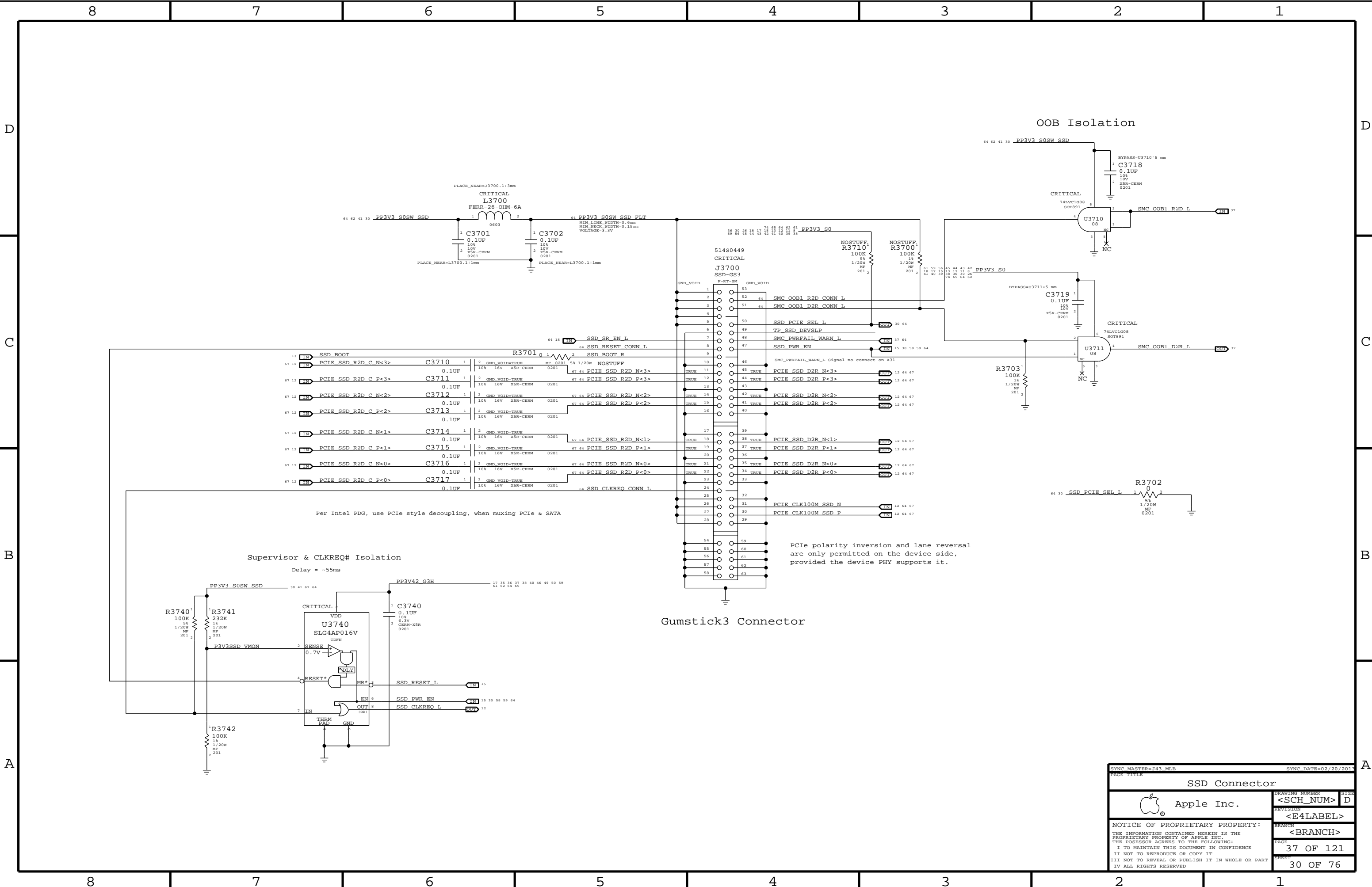
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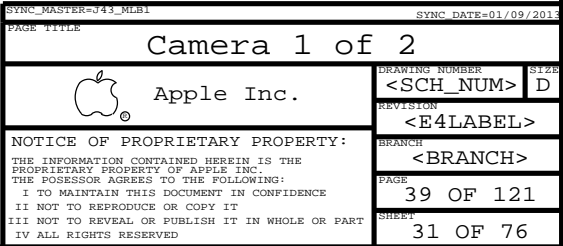
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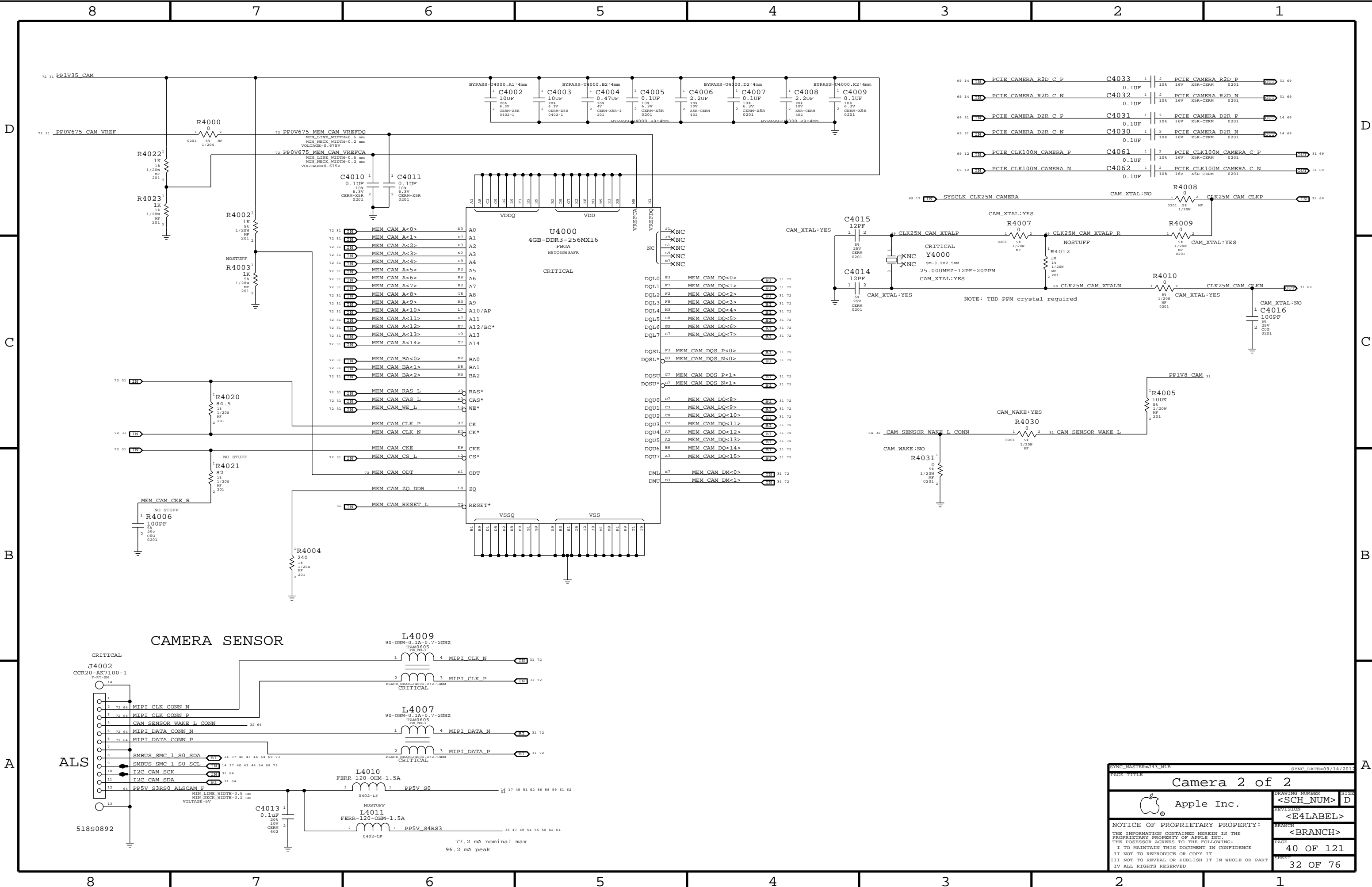
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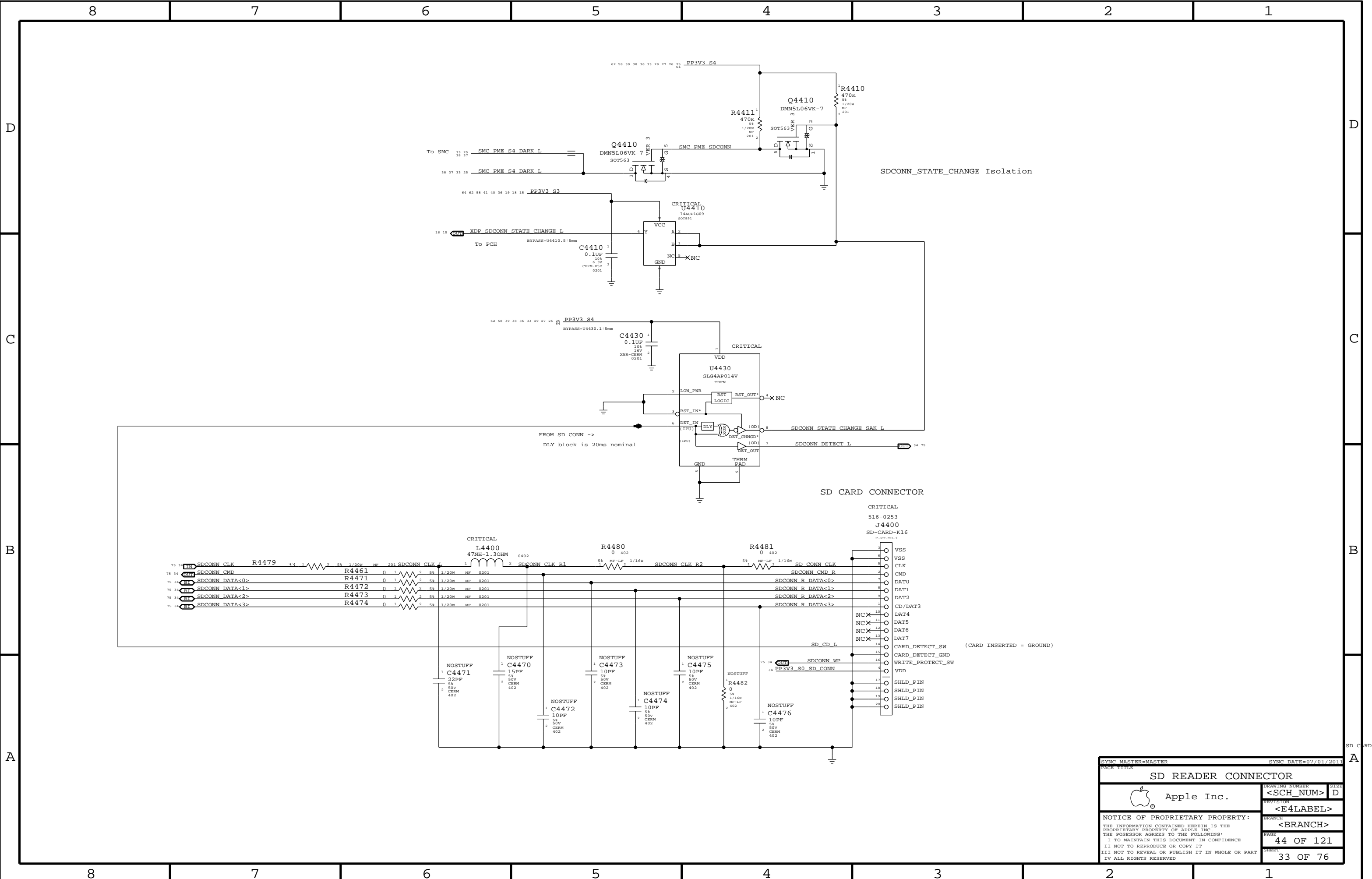
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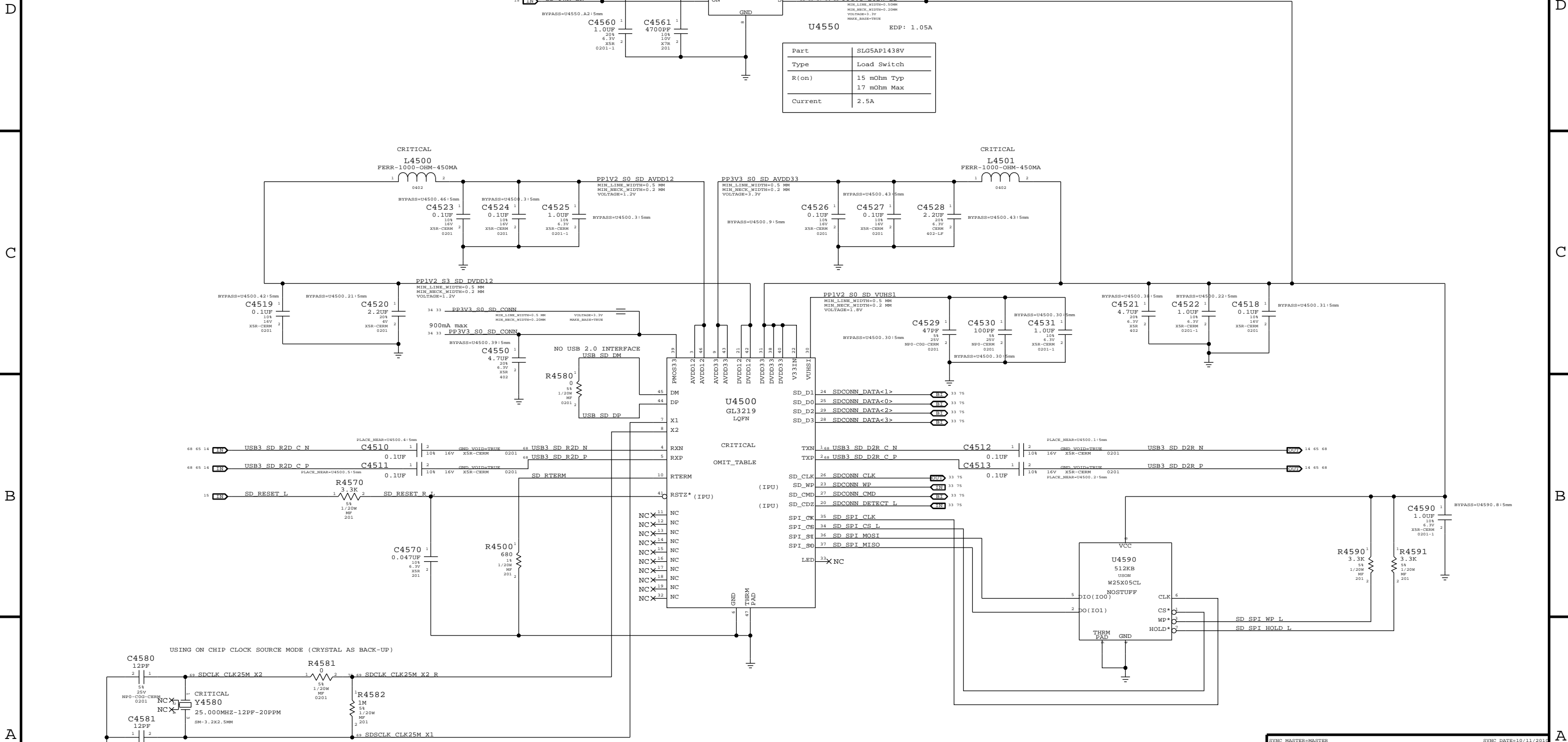






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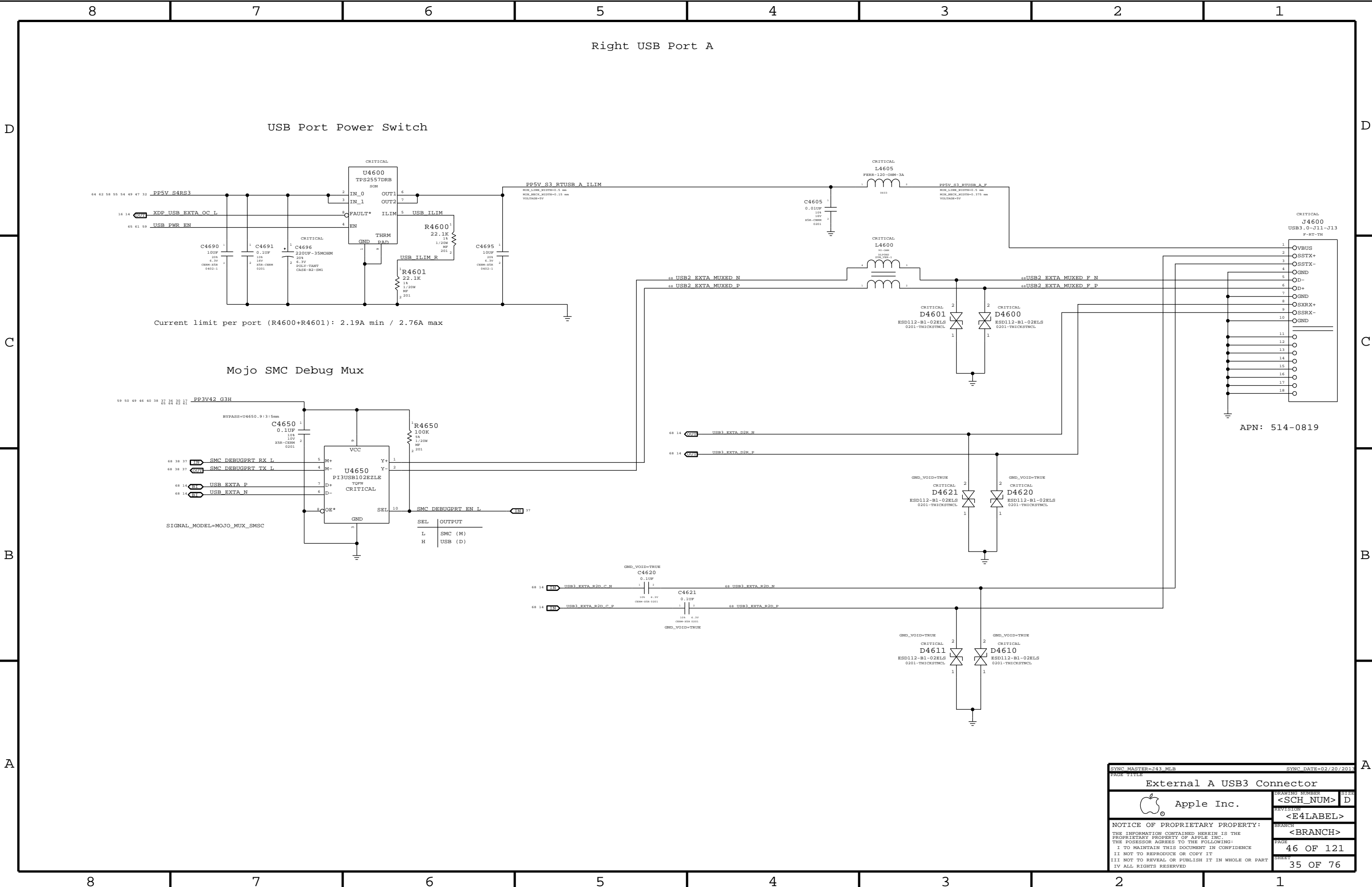


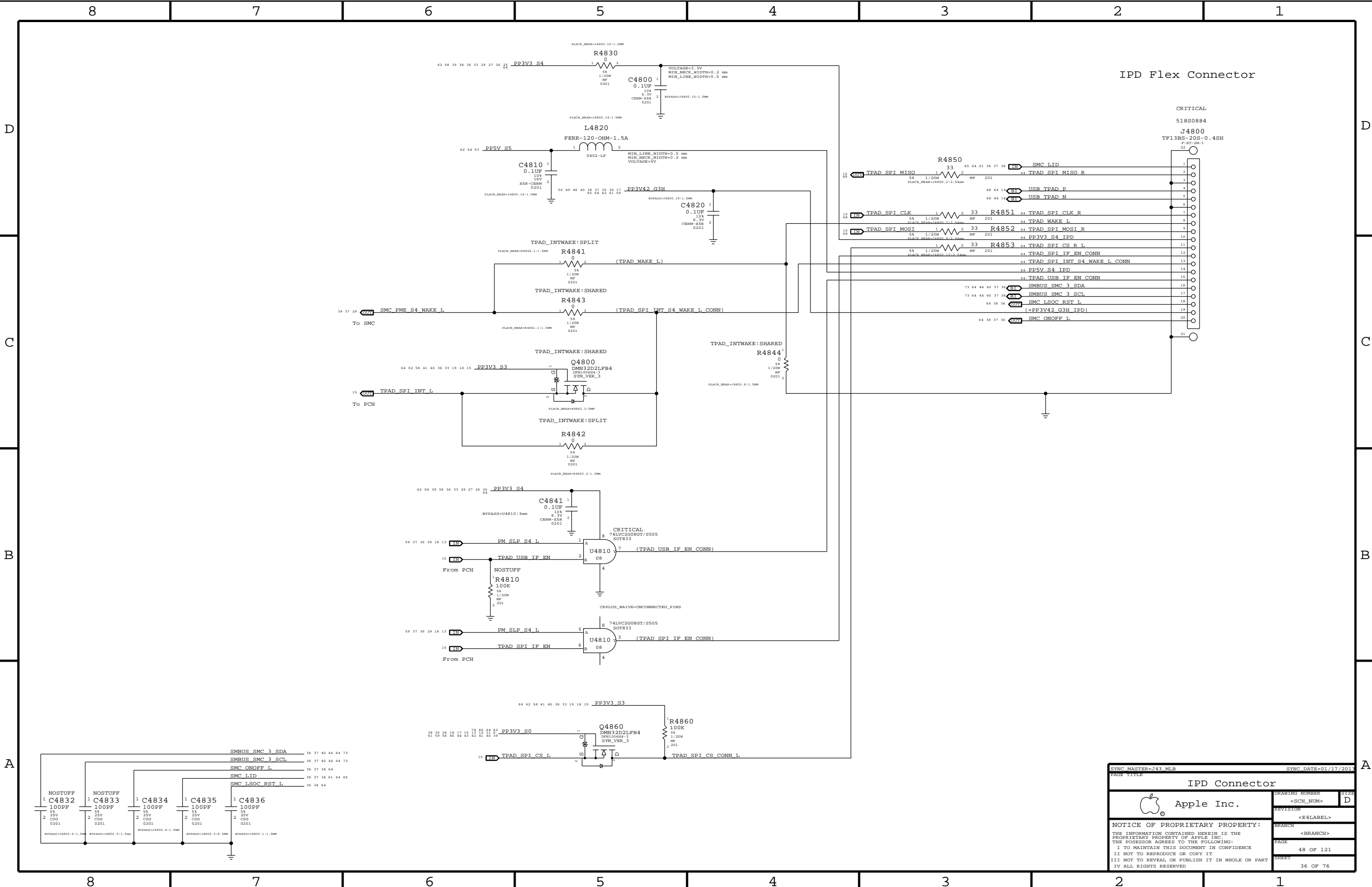
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IPD Flex Connector

CRITICAL

518S0884

J4800

TF13BS-20S-0.4SH

P-RT-SM-1

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IPD Connector



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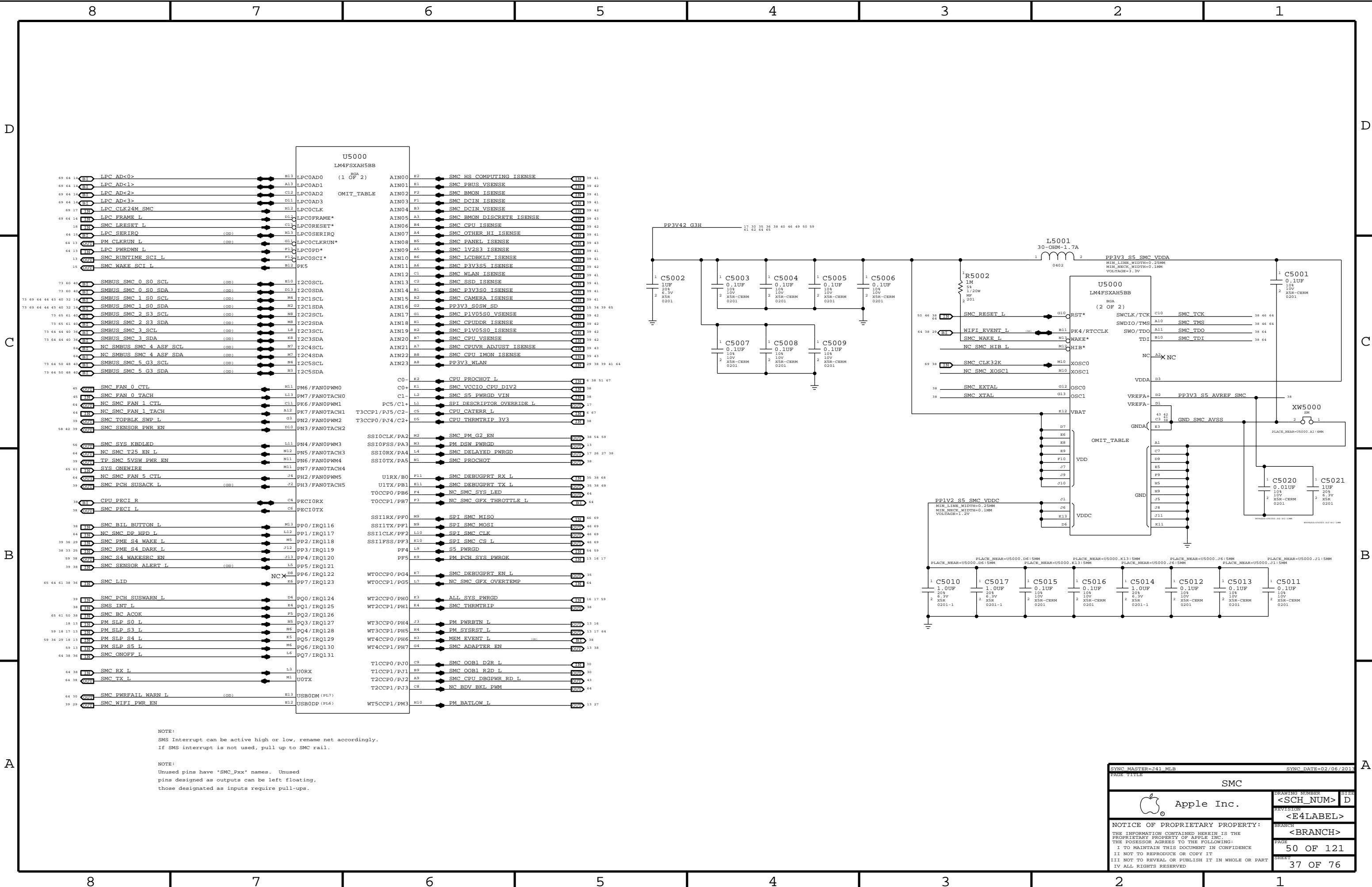
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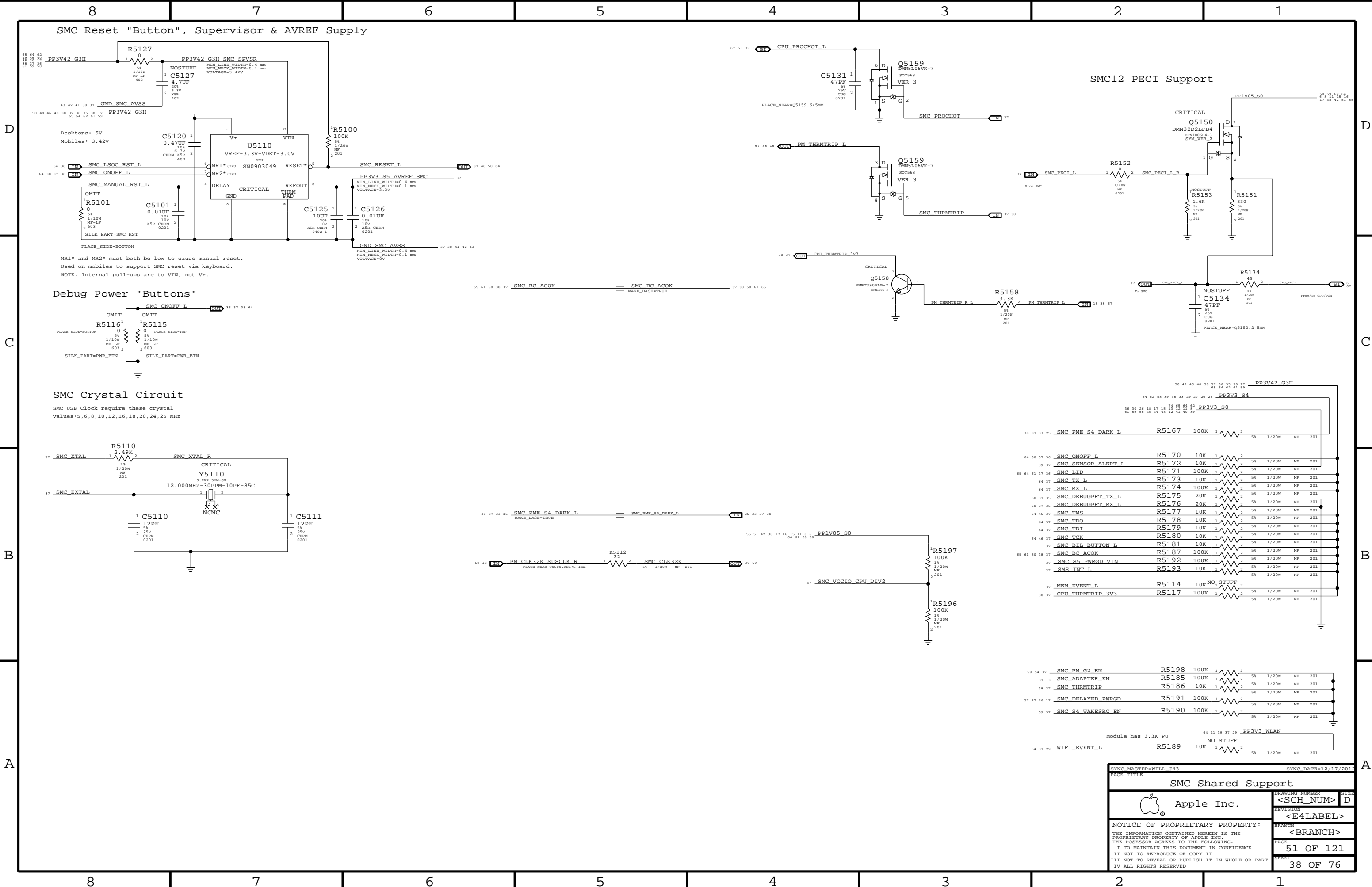
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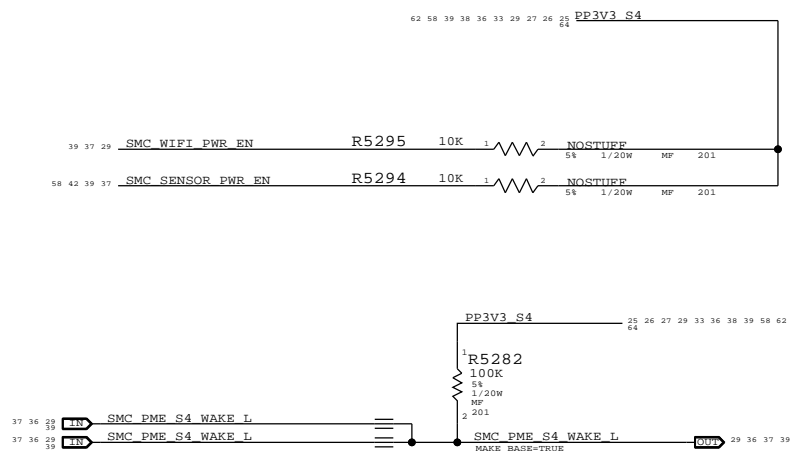
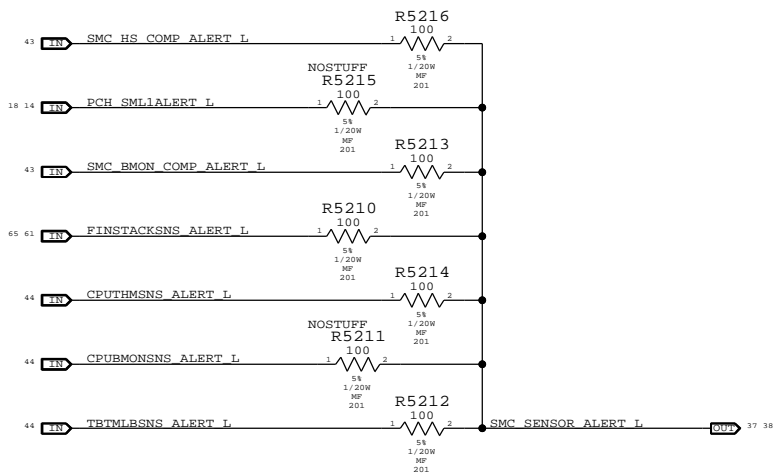
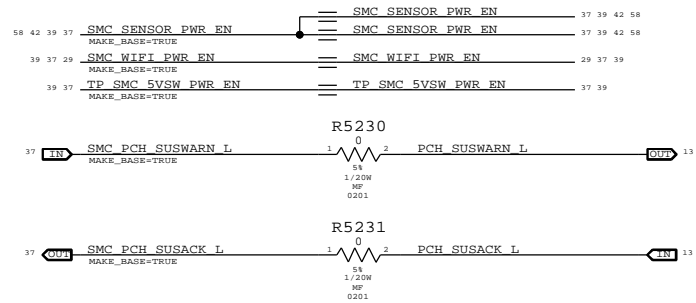
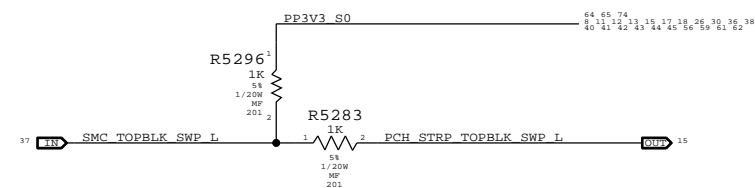


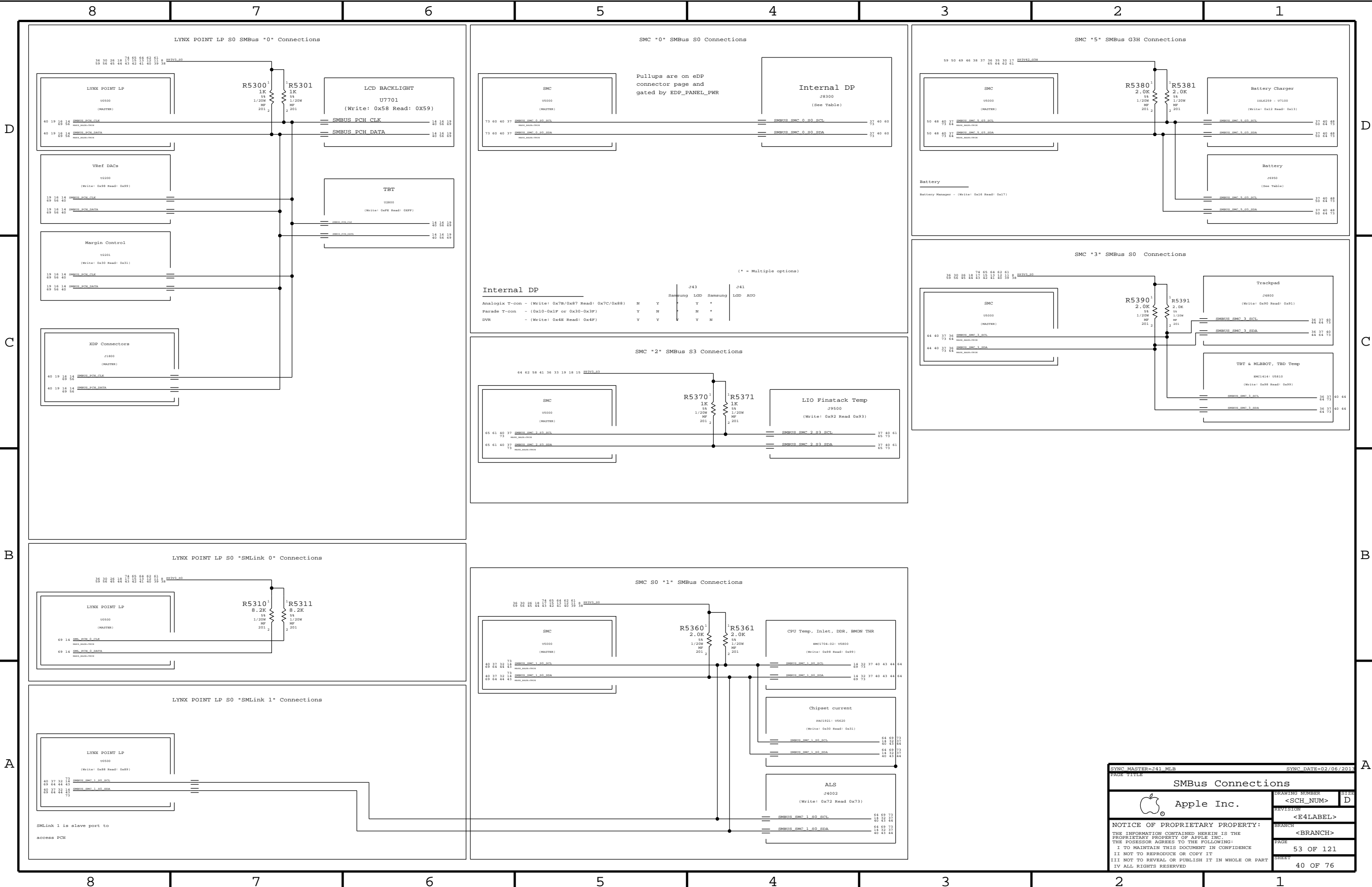
NOTE:
SMS Interrupt can be active high or low, rename net accordingly.
If SMS interrupt is not used, pull up to SMC rail.

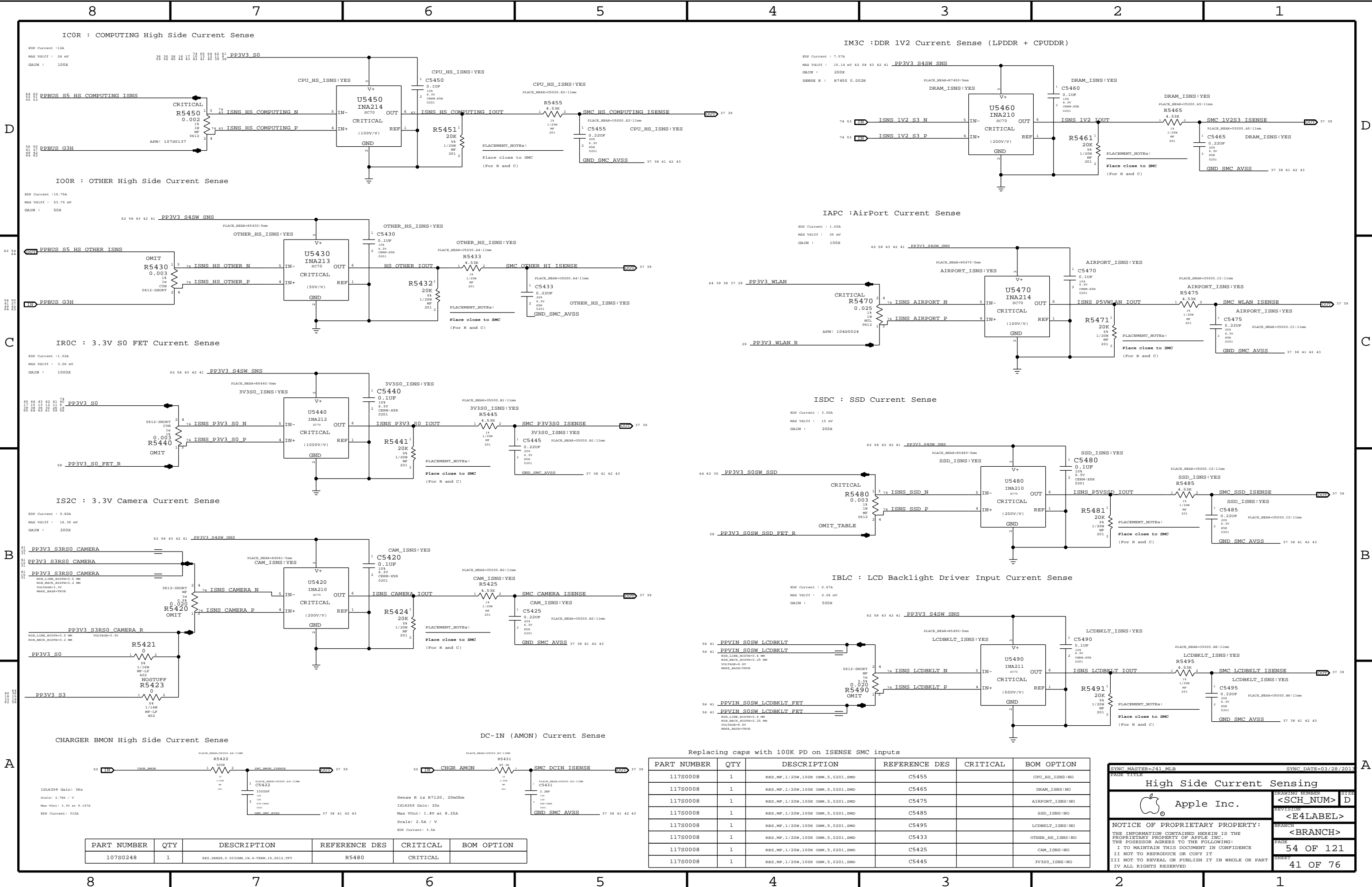
NOTE:
Unused pins have "SMC_Pxx" names. Unused
pins designed as outputs can be left floating,
those designated as inputs require pull-ups.

SYNC MASTER=J41 MLB		SYNC DATE=02/06/2013	
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SMC			
 Apple Inc.		DRAWING NUMBER	SIZE
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		REVISION	
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		BRANCH	
		<BRANCH>	
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		SHEET	37 OF 76










PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
107S0248	1	RES,SMD,R,0.0030HM,1W,4-TERM,1A,0612,TPT	R5480	CRITICAL	

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
117S0008	1	RES,MP,1/20W,100K OHM,5,0201,SMD	C5455		CPU_HS_ISNS:NO
117S0008	1	RES,MP,1/20W,100K OHM,5,0201,SMD	C5465		DRAM_ISNS:NO
117S0008	1	RES,MP,1/20W,100K OHM,5,0201,SMD	C5475		AIRPORT_ISNS:NO
117S0008	1	RES,MP,1/20W,100K OHM,5,0201,SMD	C5485		SSD_ISNS:NO
117S0008	1	RES,MP,1/20W,100K OHM,5,0201,SMD	C5495		LCDBKLT_ISNS:NO
117S0008	1	RES,MP,1/20W,100K OHM,5,0201,SMD	C5433		OTHER_HS_ISNS:NO
117S0008	1	RES,MP,1/20W,100K OHM,5,0201,SMD	C5425		CAM_ISNS:NO
117S0008	1	RES,MP,1/20W,100K OHM,5,0201,SMD	C5445		3V3S0_ISNS:NO

SYNC MASTER=J41 MLB

SYNC DATE=03/28/2013

High Side Current Sensing

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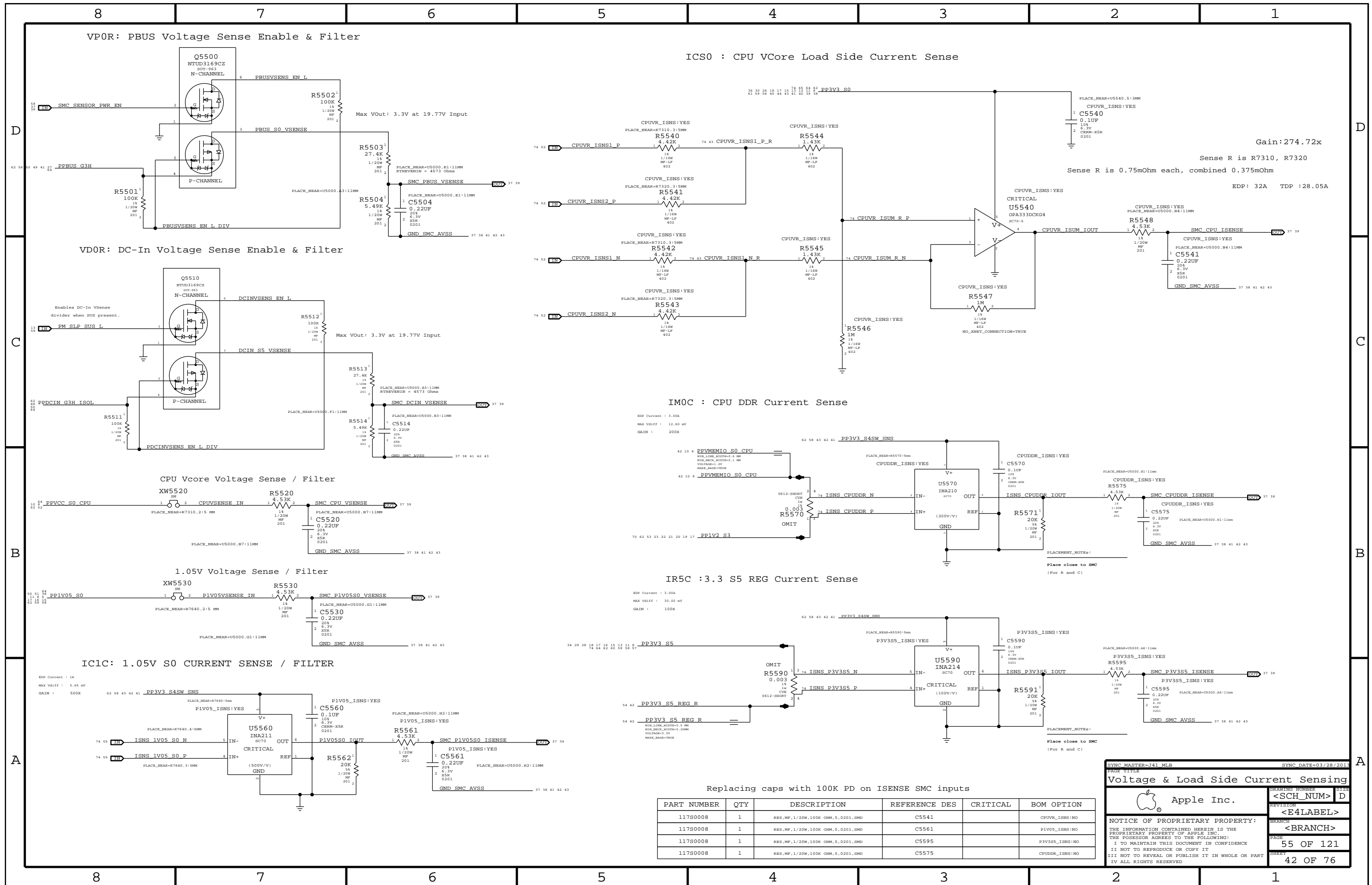
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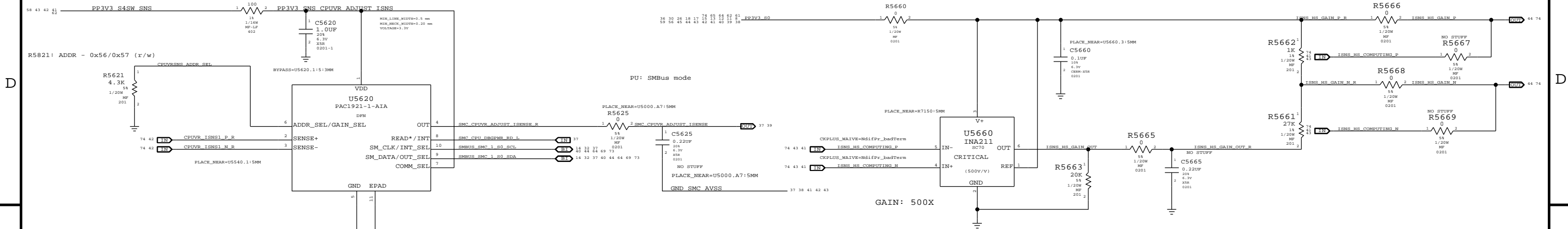
54 OF 121

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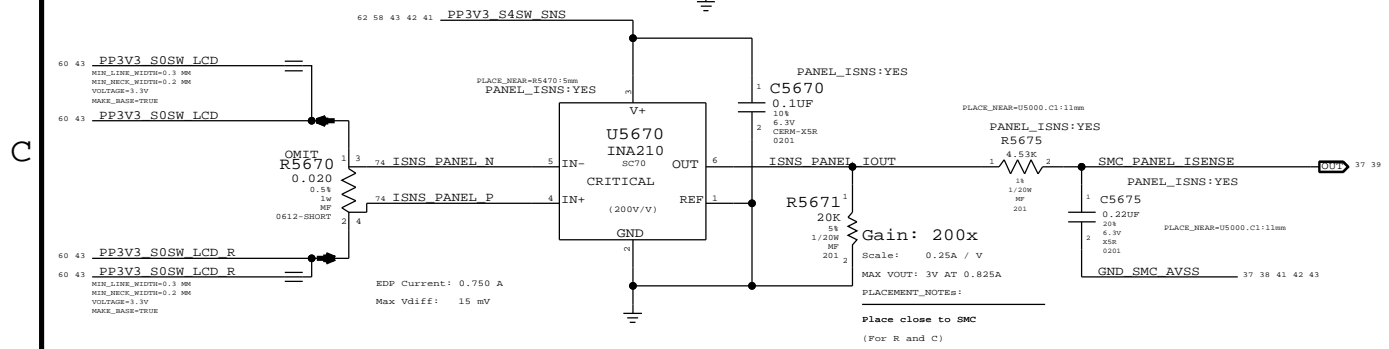


ICS3 : Adjustable Gain CPU VR Current

Sense Pins gain stage for U5800 (EMC1704)



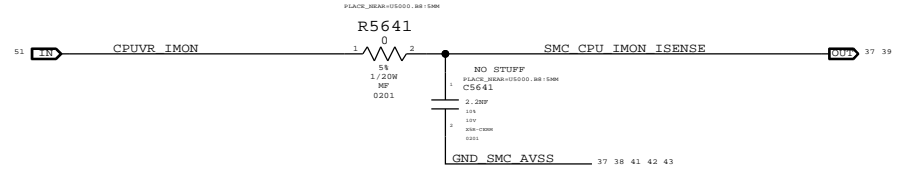
ILDC :LCD Panel Current Sense / Filter



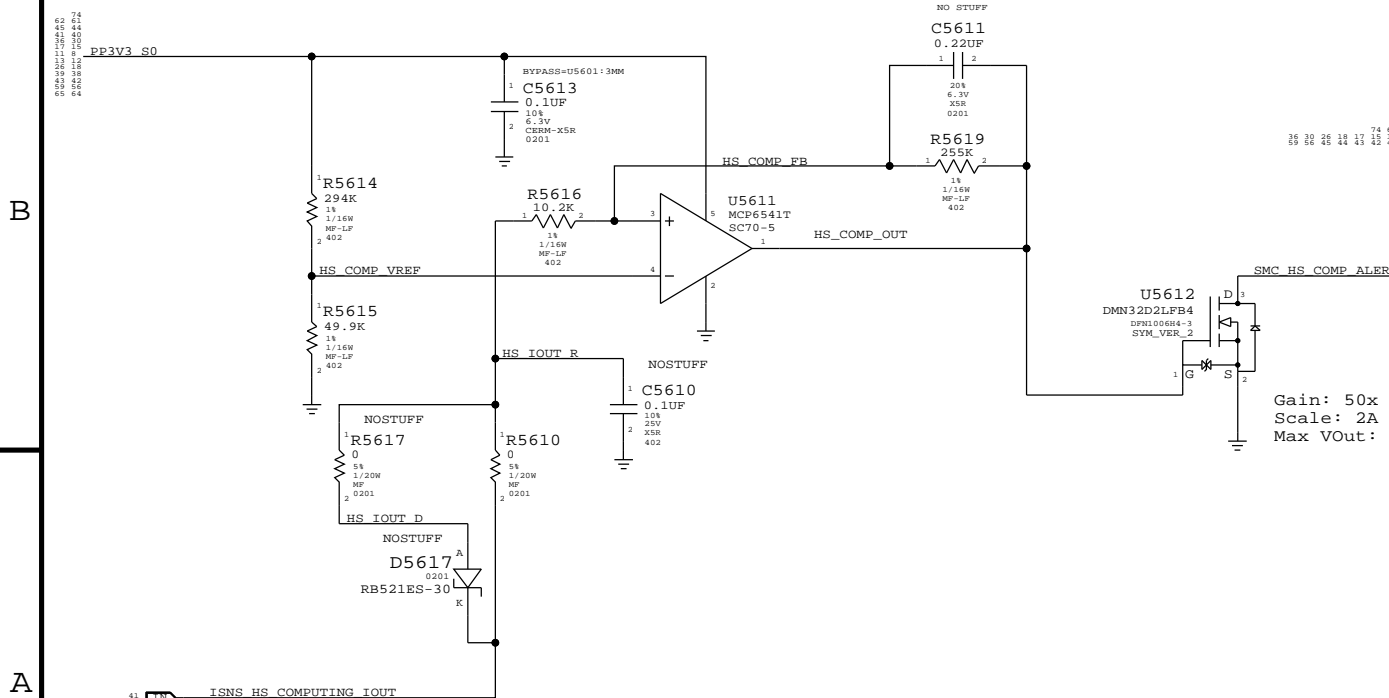
In battery discharge scenario negative voltage will be present on IN+/- pins with INA output voltage decreasing from 3.3V with increasing discharge current.

With 100mA battery current, Will have 10.2mV difference going into sense pins of U5800. This will set the mininum current threshold at 0.100mA

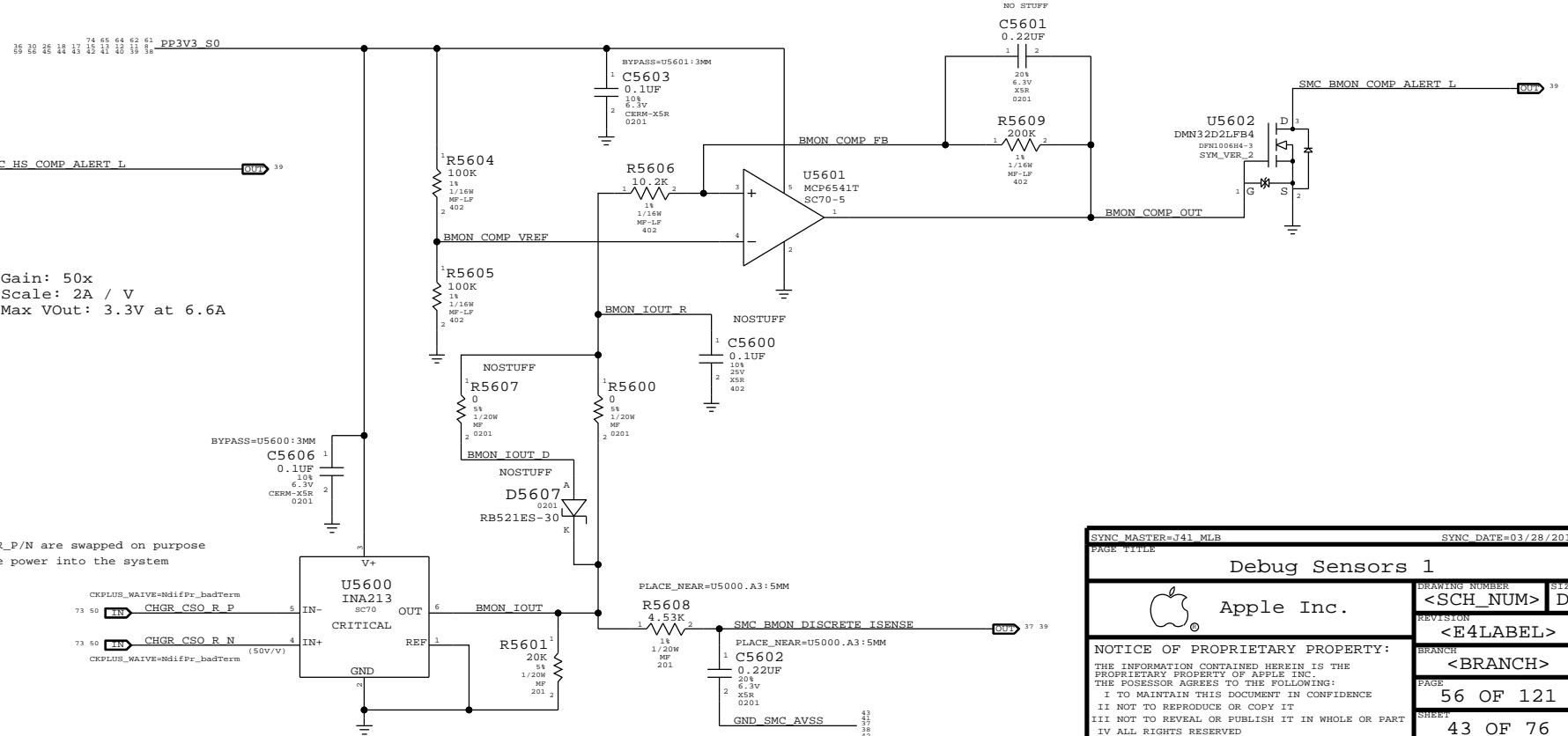
VR IMON Current Sense Filter



Discrete High side Current threshold



BMON : Discrete BMON Current Sense / Filter



Vref = 0.406mV Vth = 0.442 = 1A from Battery
Vtl = 0.290mv = 0.687A from battery
Hysteresis TBD based on RC value changes

Replacing caps with 100K PD on ISENSE SMC inputs

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
117S0008	1	RES,MP,1/20W,100K OHM,5,0201,SMD	C5675		PANEL_ISNS:NO

SYNC MASTER=J41 MLB

SYNC DATE=03/28/2013

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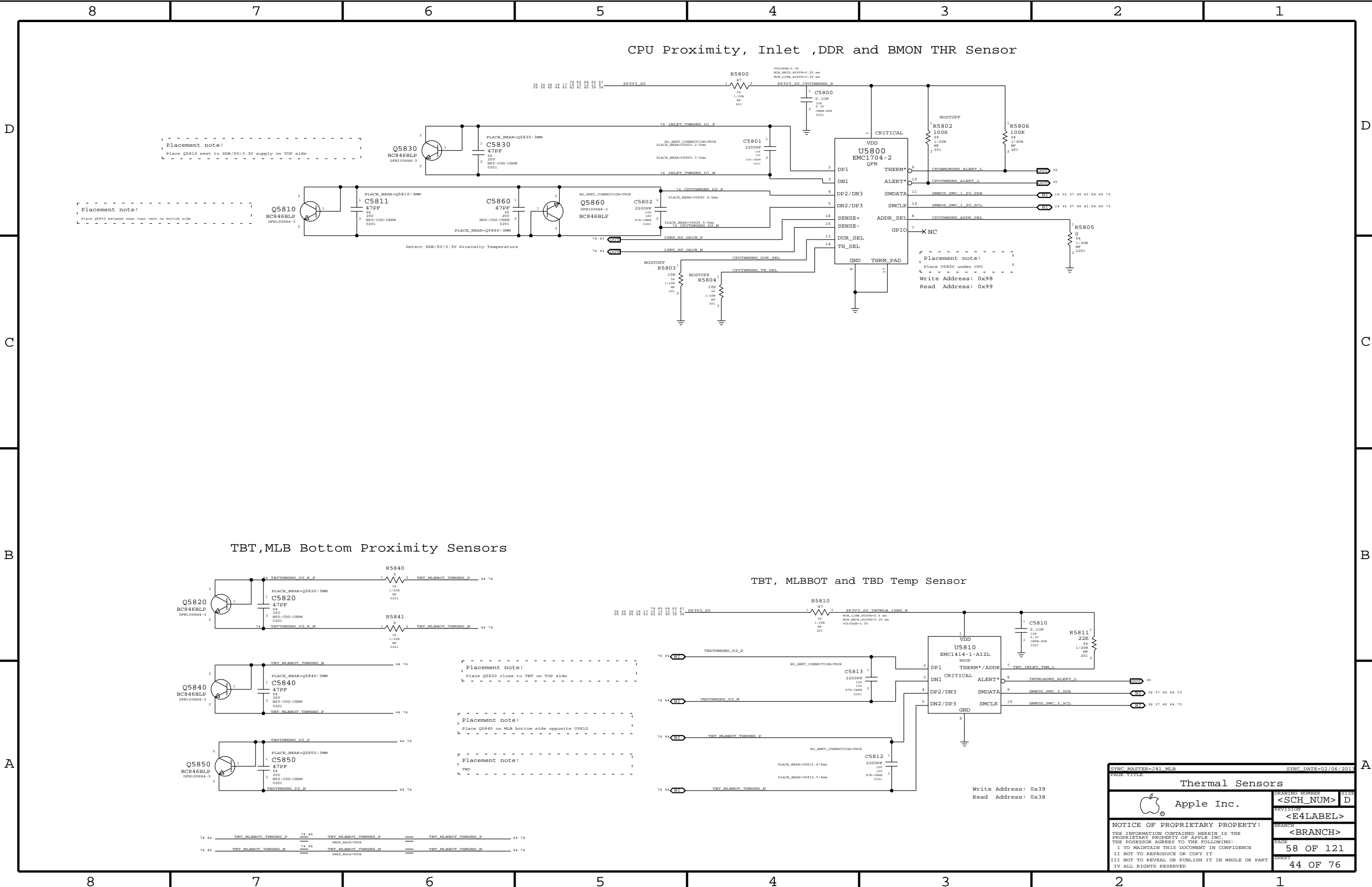
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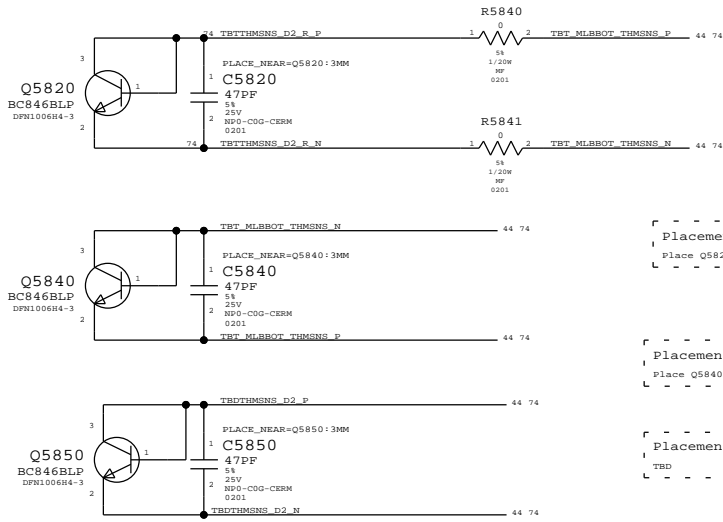
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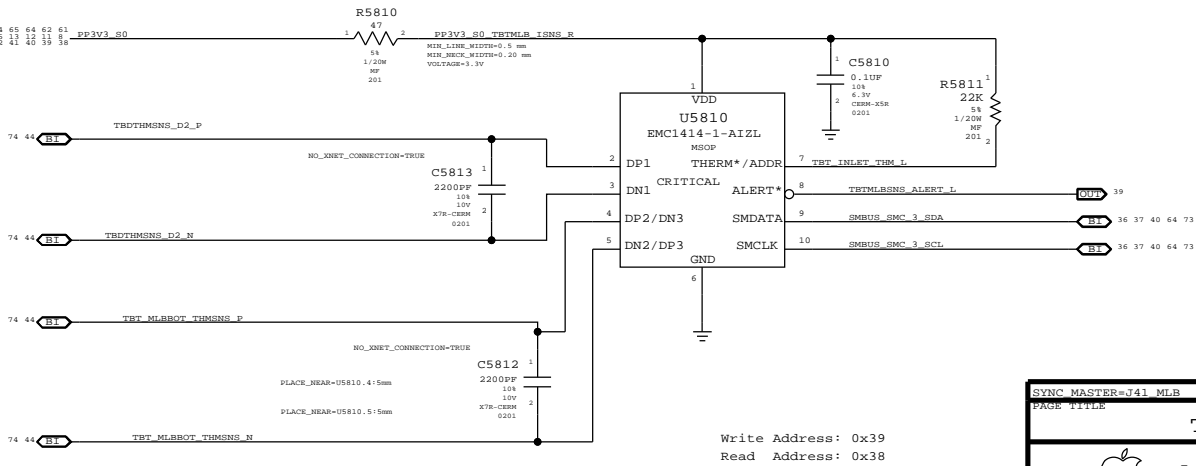
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TBT,MLB Bottom Proximity Sensors

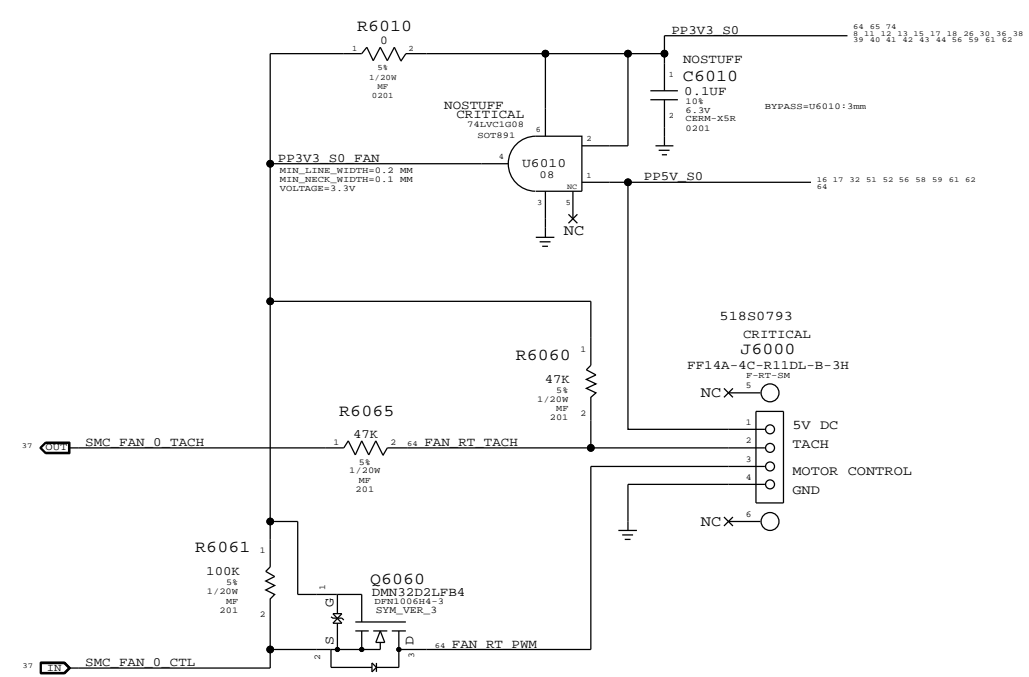


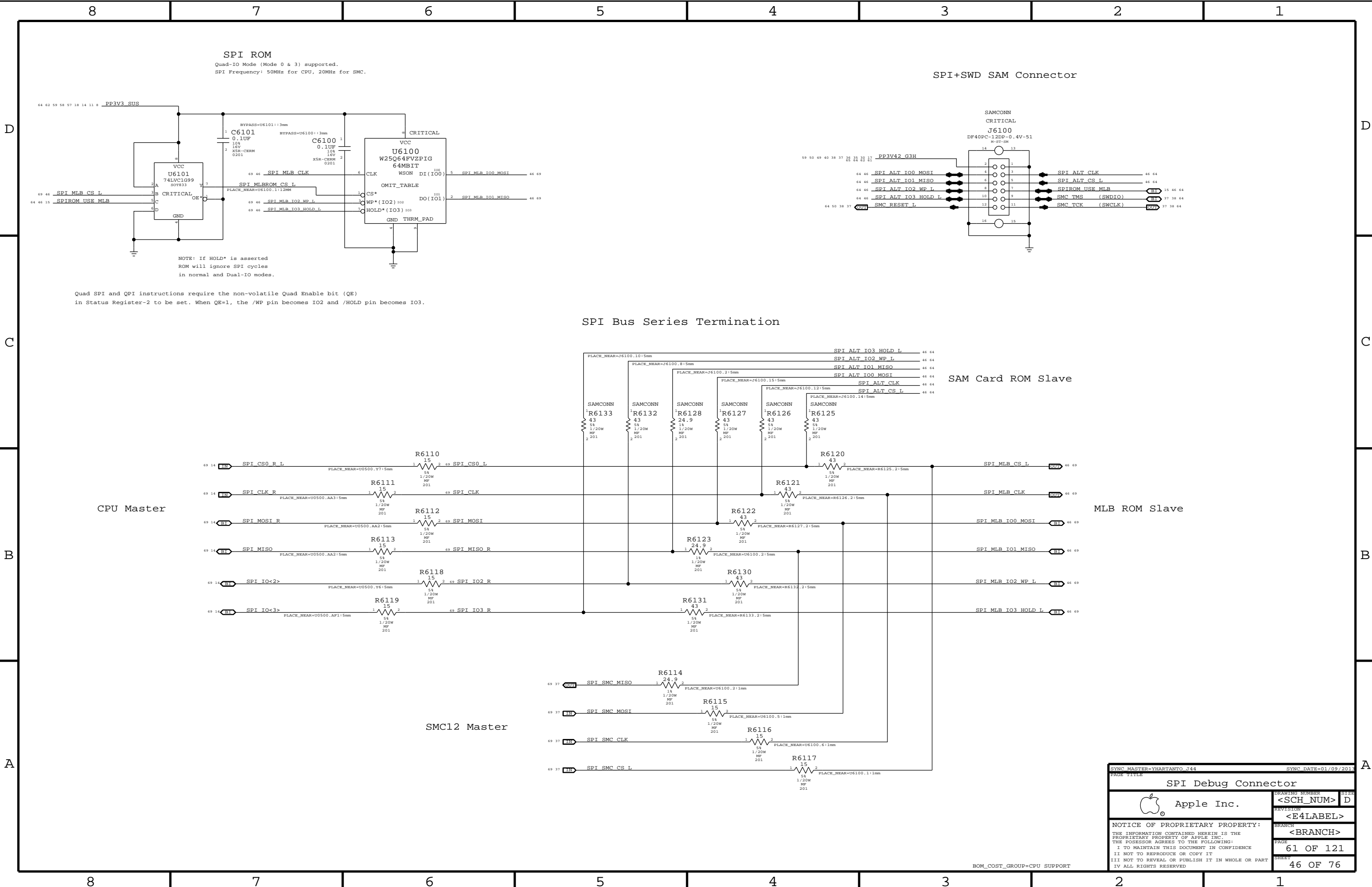
TBT, MLBBOT and TBD Temp Sensor




SYNC MASTER=J41 MLB		SYNC DATE=02/06/2013	
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Thermal Sensors			
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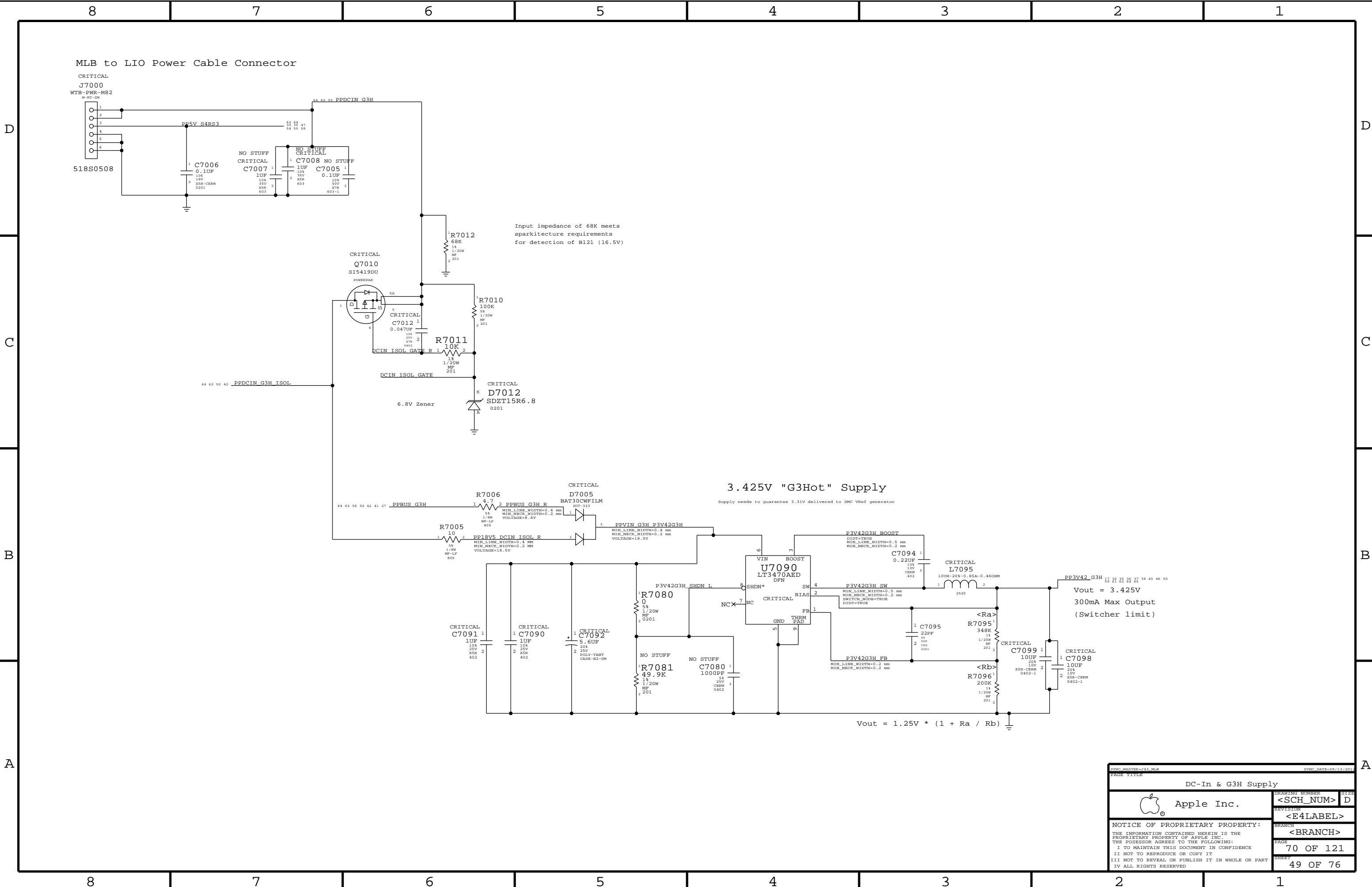
FAN CONNECTOR




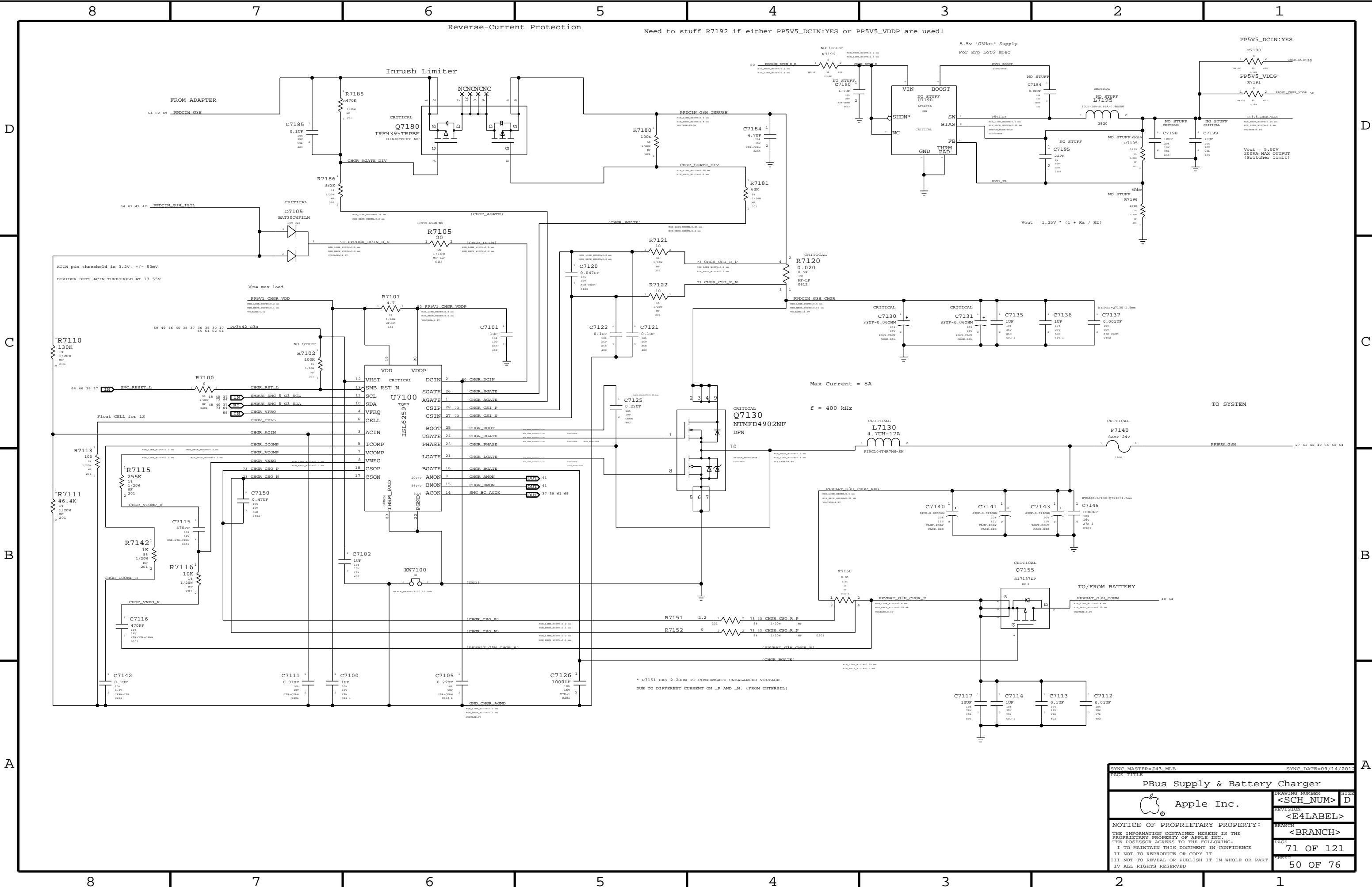



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SPI Debug Connector		DRAWING NUMBER	
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BOM_COST_GROUP=CPU SUPPORT

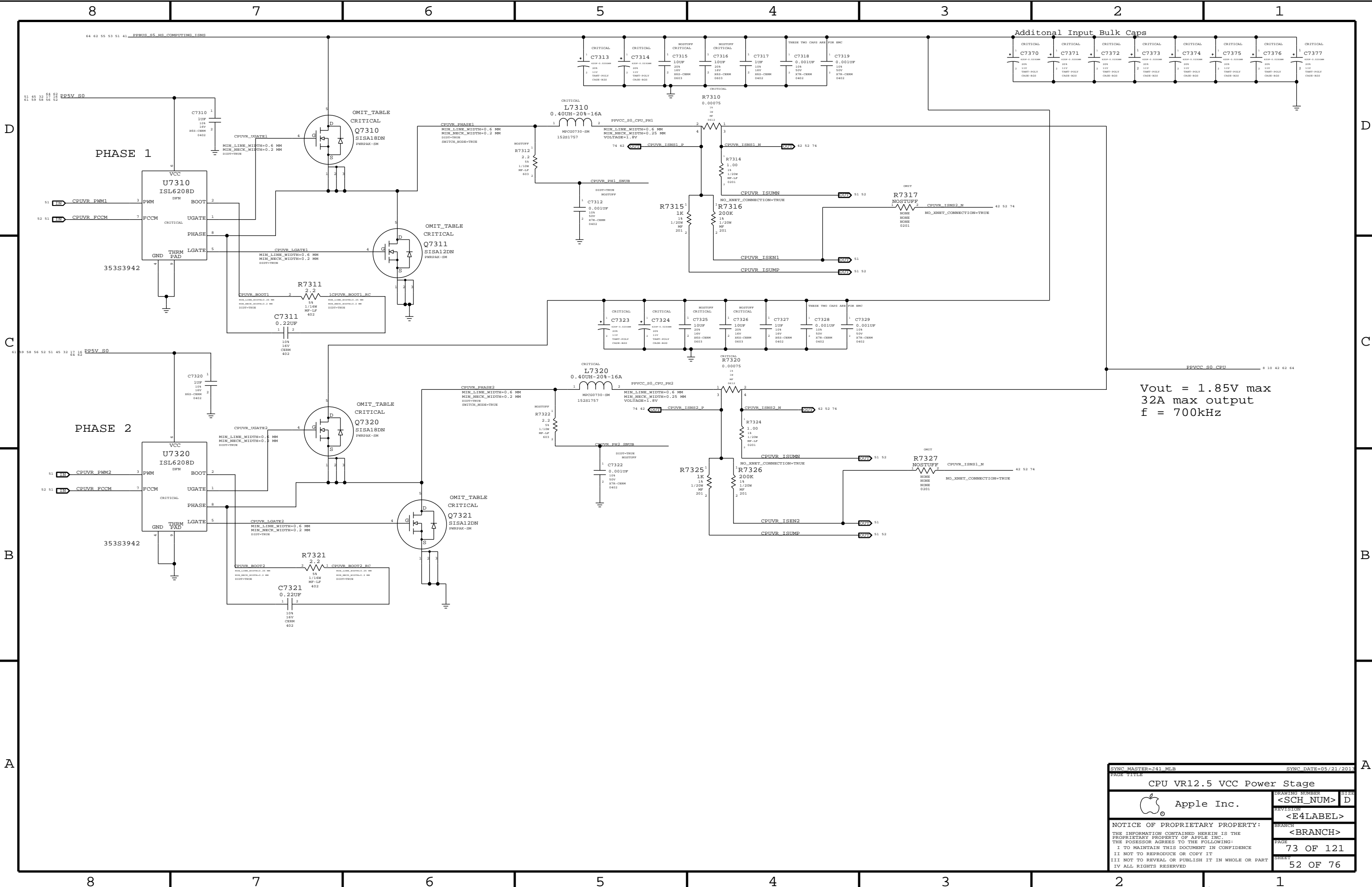



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DC-In & G3H Supply			
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SYNC MASTER=J43 MLB		SYNC DATE=09/14/2012	
PAGE TITLE			
PBus Supply & Battery Charger			
 Apple Inc.		DRAWING NUMBER	SIZE
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CPU VR12.5 VCC Power Stage			
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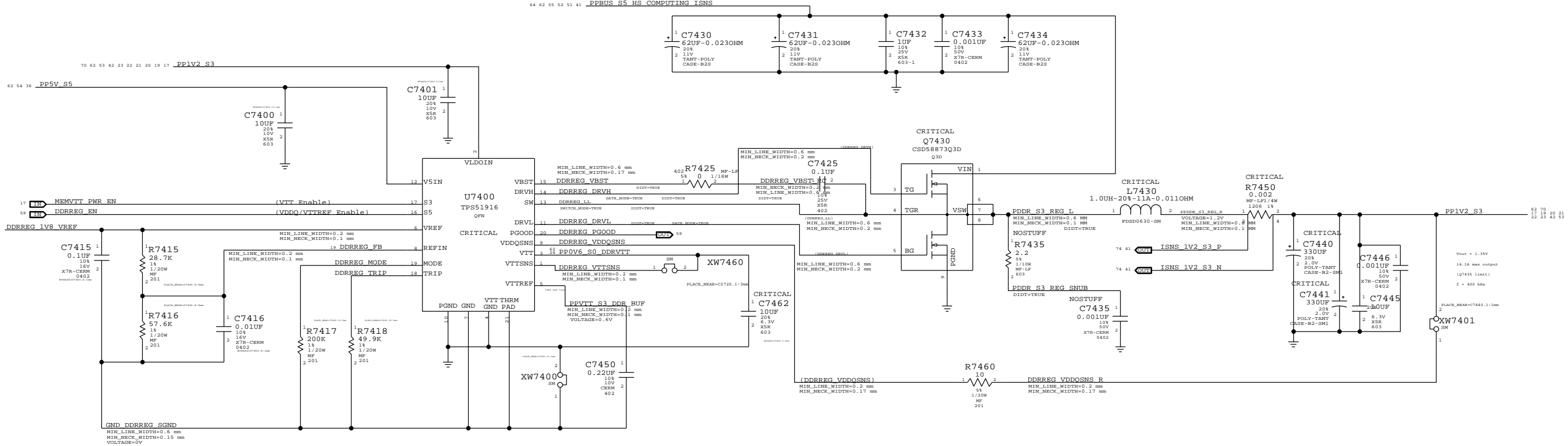
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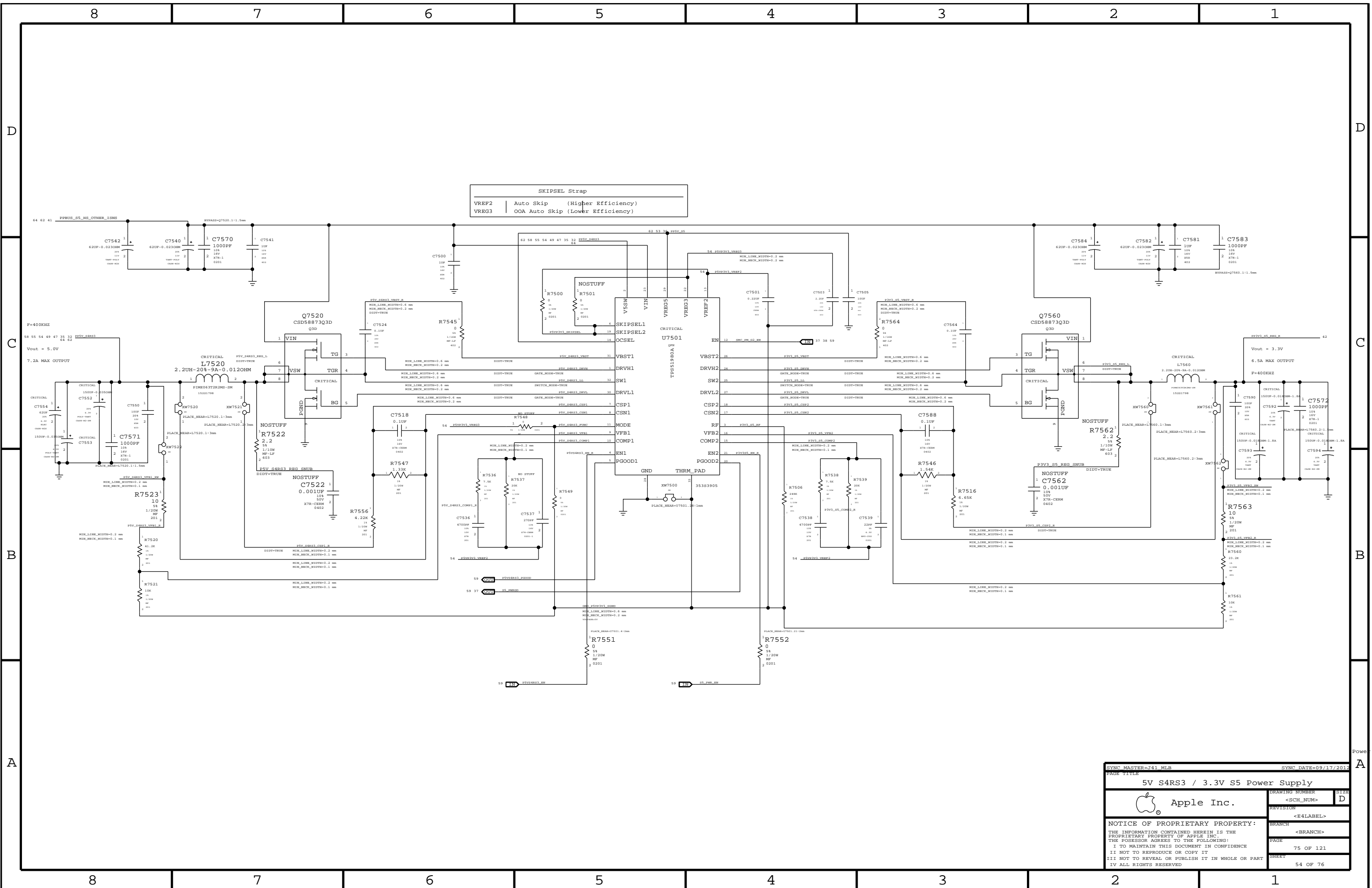
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
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5V S4RS3 / 3.3V S5 Power Supply			
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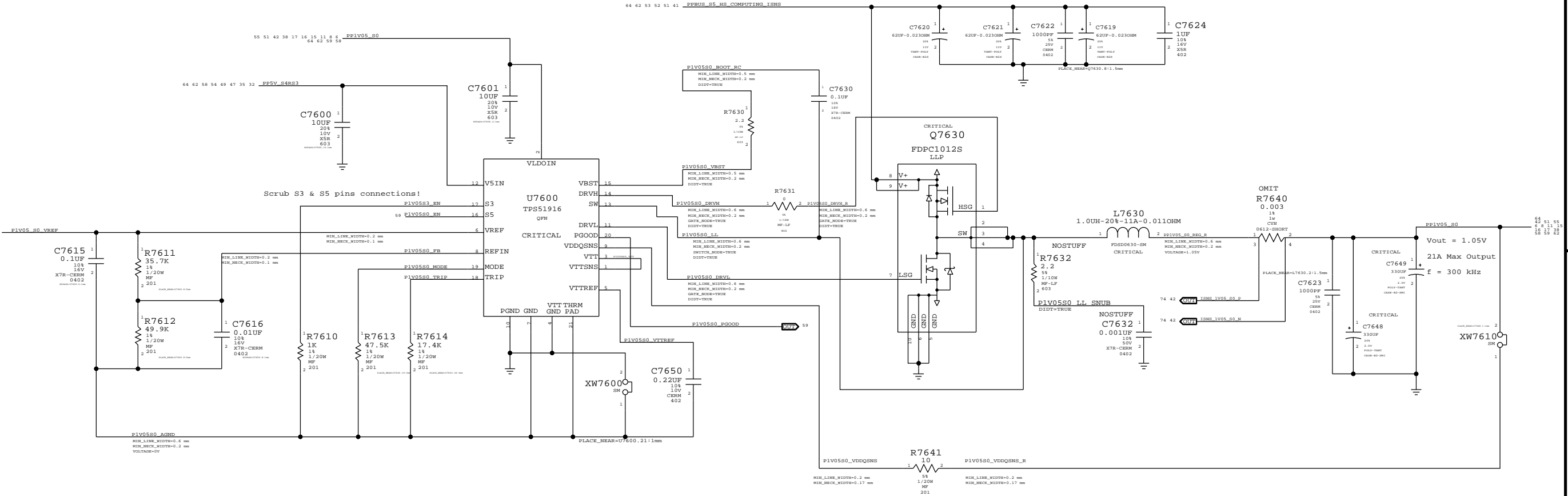
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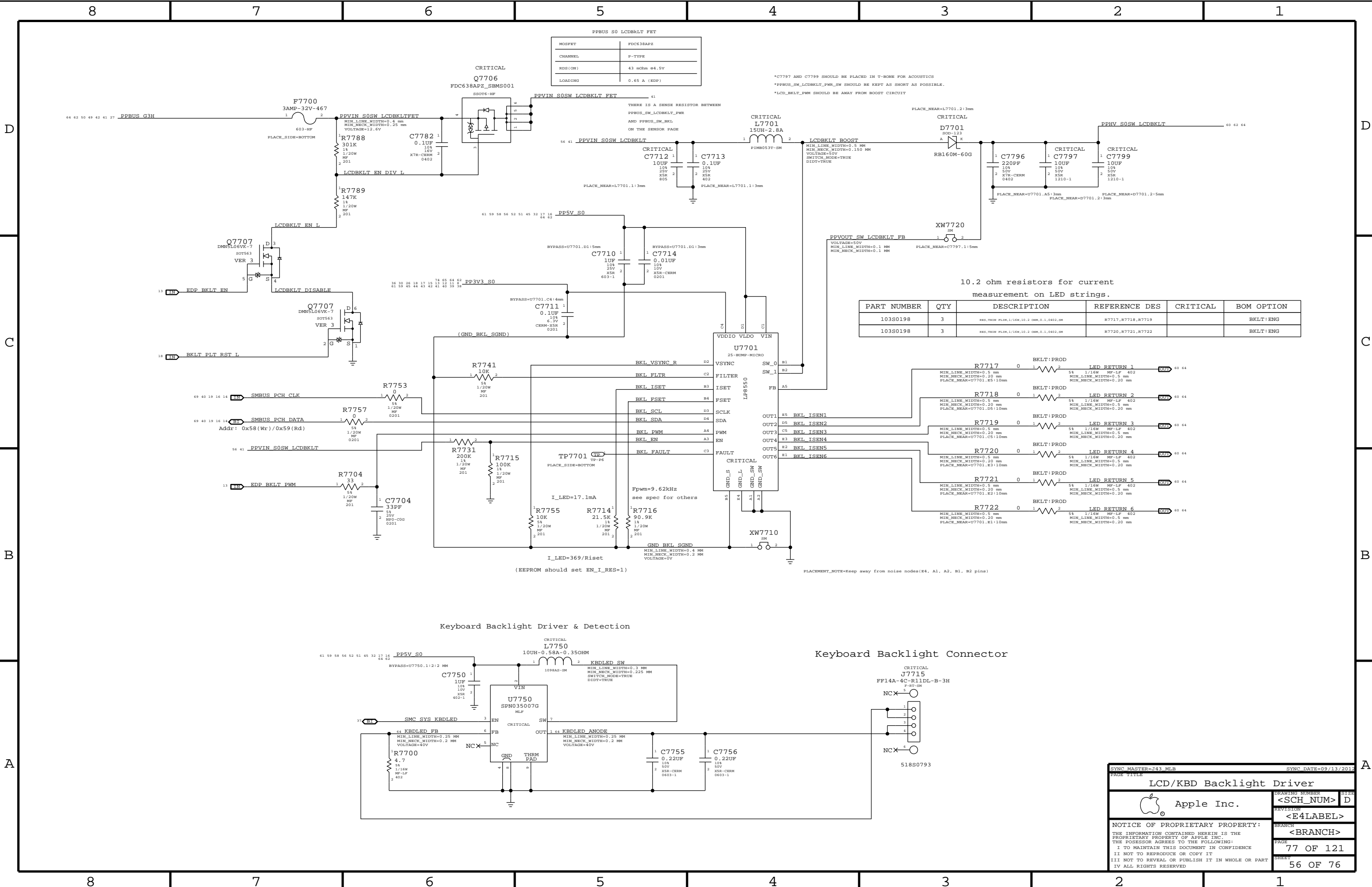
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1.05V S0 Regulator



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1.05V S0 Power Supply			
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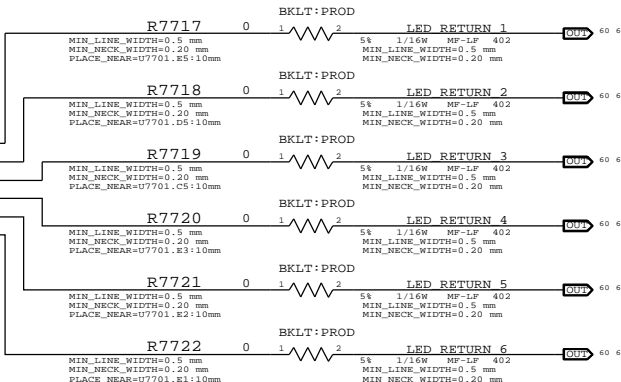
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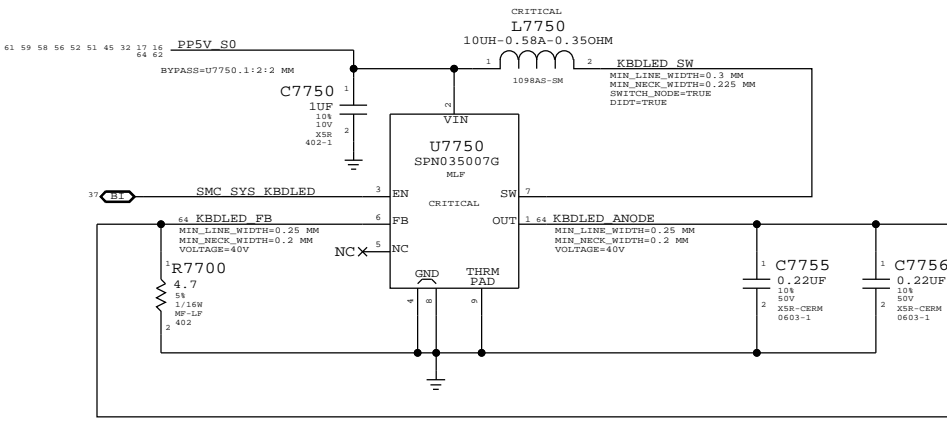
PPBUS S0 LCDBKLT FET	
MOSFET	FDC638APZ
CHANNEL	P-TYPE
RDS(ON)	43 mOhm @4.5V
LOADING	0.65 A (RDP)

*C7797 AND C7799 SHOULD BE PLACED IN T-BONE FOR ACOUSTICS
*PPBUS_SW_LCDBKLT_PWR_SW SHOULD BE KEPT AS SHORT AS POSSIBLE.
*LCD_BKLT_PWM SHOULD BE AWAY FROM BOOST CIRCUIT

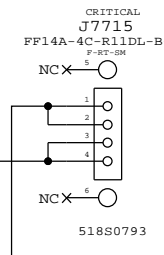
PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
103S0198	3	RES,THIN FILM,I/16W,10.2 OHM,0.1,0402,SM	R7717,R7718,R7719		BKLT:ENG
103S0198	3	RES,THIN FILM,I/16W,10.2 OHM,0.1,0402,SM	R7720,R7721,R7722		BKLT:ENG




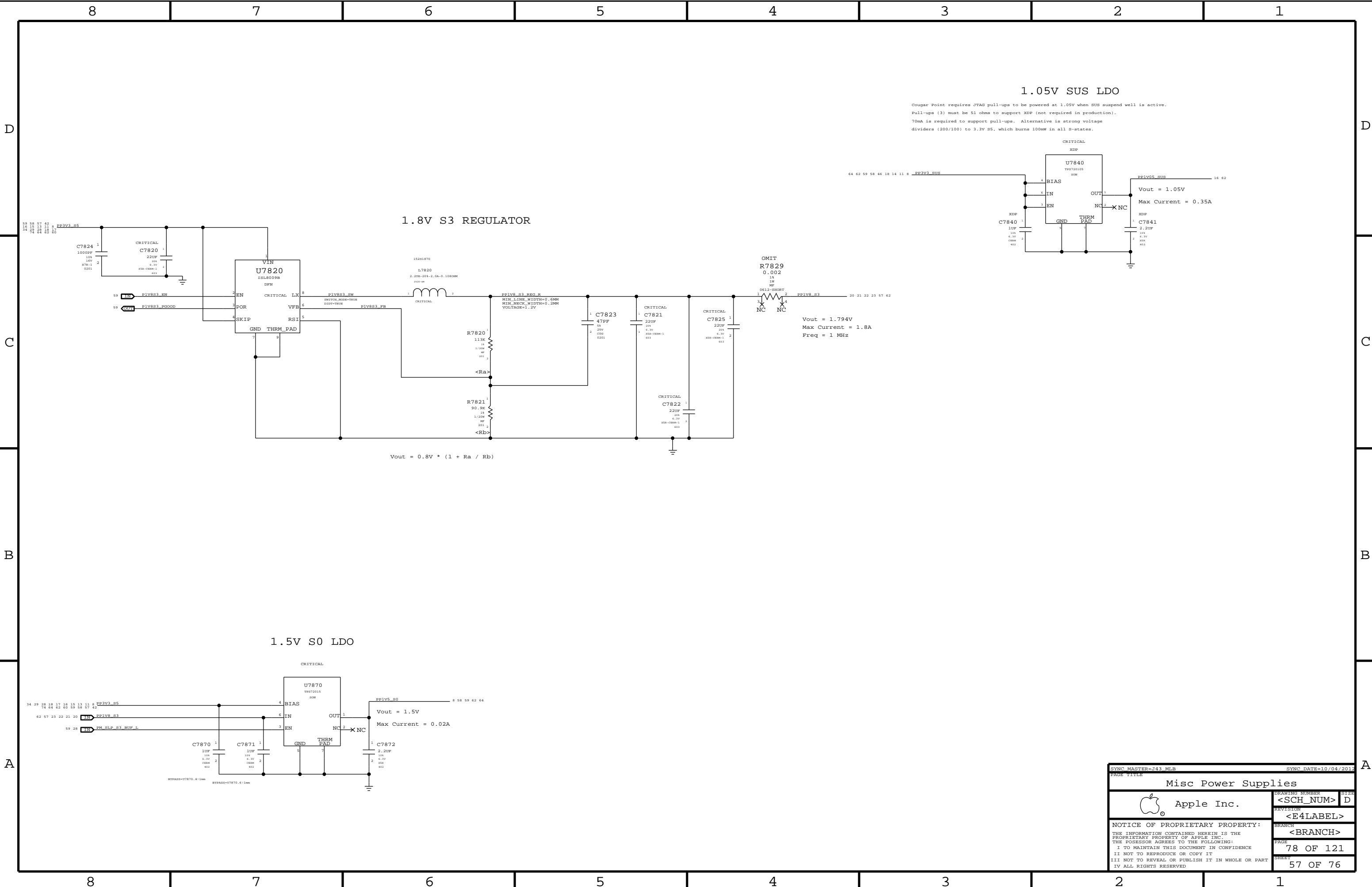
Keyboard Backlight Driver & Detection




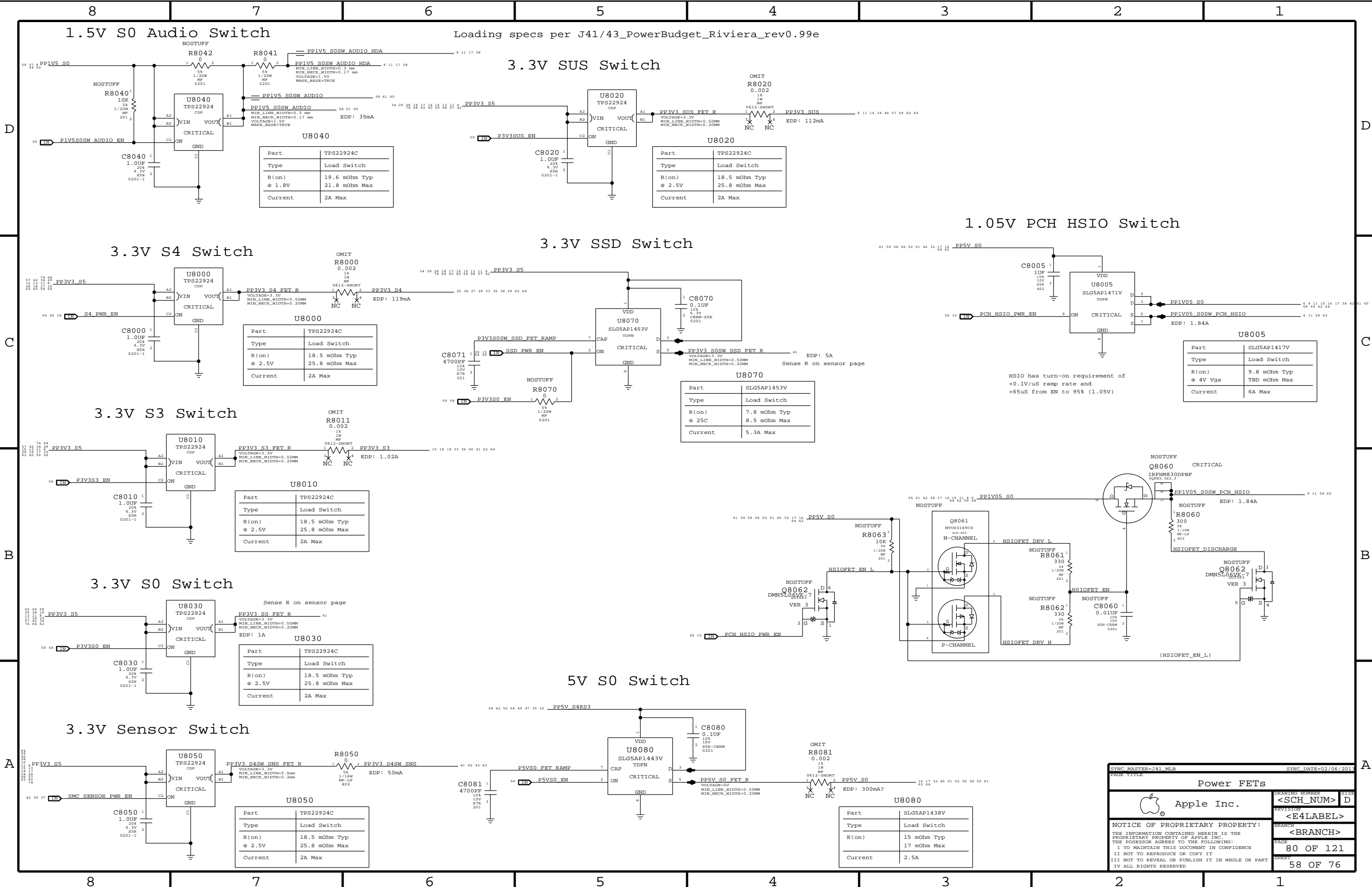
Keyboard Backlight Connector



SYNC MASTER=J43 MLB		SYNC DATE=09/13/2012	
PAGE TITLE			
LCD/KBD Backlight Driver		DRAWING NUMBER	SIZE
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PAGE TITLE			
Misc Power Supplies			
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Loading specs per J41/43_PowerBudget_Riviera_rev0.99e

1.5V S0 Audio Switch

3.3V SUS Switch

1.05V PCH HSIO Switch

5V S0 Switch

3.3V Sensor Switch

3.3V S4 Switch

3.3V SSD Switch

3.3V S3 Switch

3.3V S0 Switch

Part	TPS22924C
Type	Load Switch
R(on) @ 1.8V	19.6 mOhm Typ 21.8 mOhm Max
Current	2A Max

Part	TPS22924C
Type	Load Switch
R(on) @ 2.5V	18.5 mOhm Typ 25.8 mOhm Max
Current	2A Max

Part	SLG5AP1417V
Type	Load Switch
R(on) @ 4V Vgs	9.8 mOhm Typ TBD mOhm Max
Current	6A Max

Part	SLG5AP1453V
Type	Load Switch
R(on) @ 25C	7.8 mOhm Typ 8.5 mOhm Max
Current	5.3A Max

Part	TPS22924C
Type	Load Switch
R(on) @ 2.5V	18.5 mOhm Typ 25.8 mOhm Max
Current	2A Max

Part	TPS22924C
Type	Load Switch
R(on) @ 2.5V	18.5 mOhm Typ 25.8 mOhm Max
Current	2A Max

Part	SLG5AP1438V
Type	Load Switch
R(on)	15 mOhm Typ 17 mOhm Max
Current	2.5A

Power FETs

Apple Inc.

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REVISION
<E4LABEL>

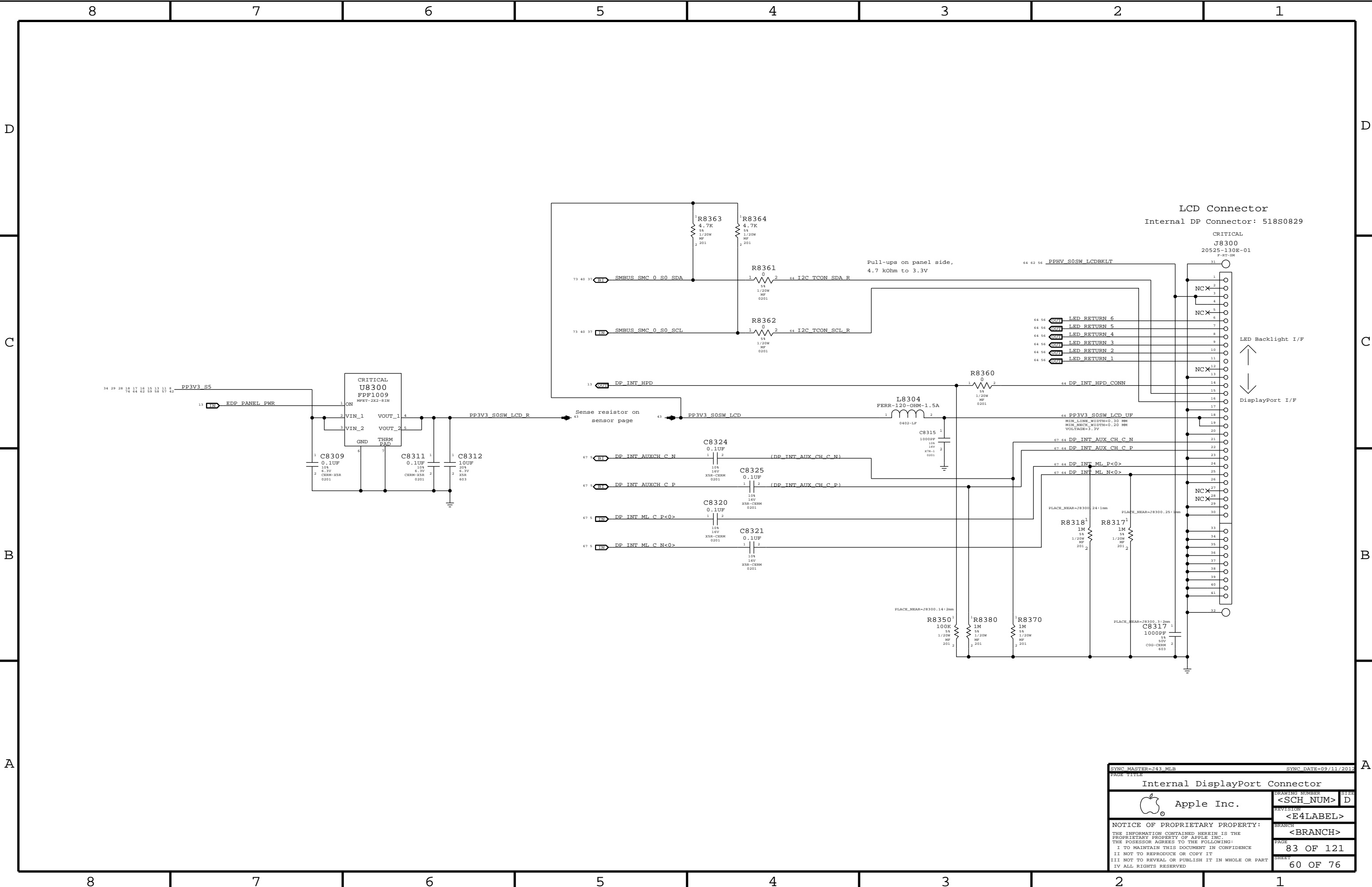
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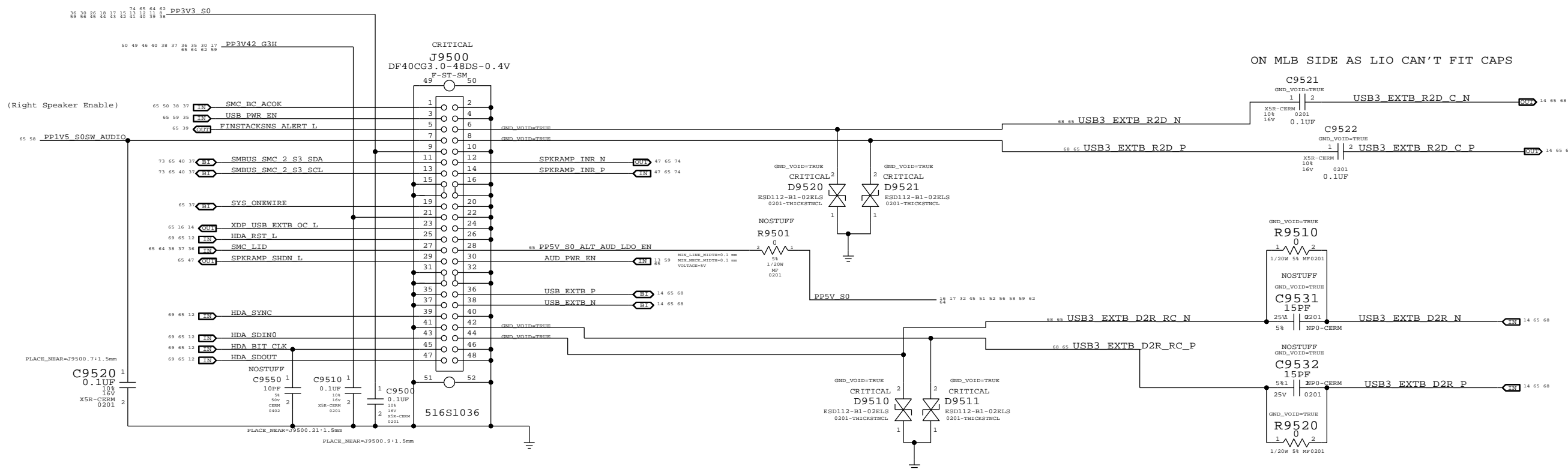
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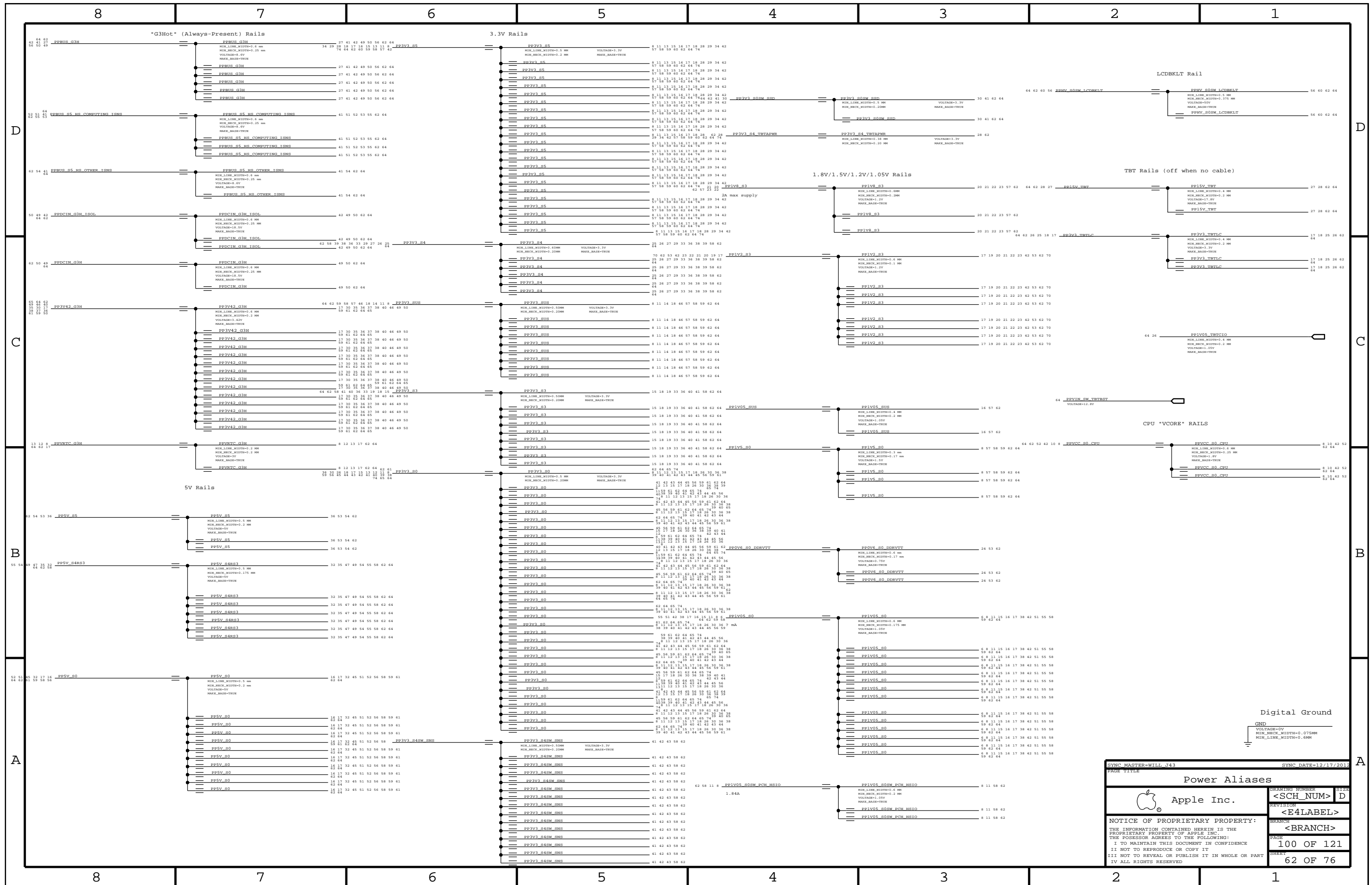
SYNC MASTER=J41 MLB

SYNC DATE=03/06/2013



SYNC MASTER=J43 MLB		SYNC DATE=09/11/2012	
PAGE TITLE			
Internal DisplayPort Connector		DRAWING NUMBER	
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Functional Test Points

NO_TEST Nets

J3501: AirPort / BT Connector

J6000: Fan Connector

Misc Voltages & Control Signals

FUNC_TEST		(Need 6 TPs)	
TRUE	PP3V3 WLAN	29	37 38 39 41
TRUE	WIFI EVENT L	29	37 38
TRUE	PCIE AP R2D N	29	69
TRUE	PCIE AP R2D P	29	69
TRUE	PCIE CLK100M AP N	12	29 69
TRUE	PCIE CLK100M AP P	12	29 69
TRUE	PCIE AP D2R P	14	29 69
TRUE	PCIE AP D2R N	14	29 69
TRUE	PCIE WAKE L	13	29 31
TRUE	AP RESET CONN L	29	
TRUE	AP CLKREQ Q L	29	
TRUE	USB BT CONN P	29	68
TRUE	USB BT CONN N	29	68
TRUE	PP3V3 S4	25	26 27 29 33 36 38
(Need to add 8 GND TPs)			

J3700: SSD Connector

FUNC_TEST		(Need 5 TPs)	
TRUE	PP3V3 S0SW SSD FLT	30	
TRUE	PCIE SSD R2D N<3..0>	30	67
TRUE	PCIE SSD R2D P<3..0>	30	67
TRUE	PP3V3 S0	62	63 64 44 45 56 59 61
TRUE	SSD RESET CONN L	8	11 25 26 38 39 40 41
TRUE	SSD CLKREQ CONN L	62	64 65 74 30
TRUE	SMC OOB1 R2D CONN L	30	
TRUE	SMC OOB1 D2R CONN L	30	
TRUE	SSD PCIE SEL L	30	
TRUE	SSD SR EN L	15	30
TRUE	SMC PWRFAIL WARN L	30	37
TRUE	SSD PWR EN	15	30 58 59
TRUE	PCIE SSD D2R N<3..0>	12	30 67
TRUE	PCIE SSD D2R P<3..0>	12	30 67
TRUE	PCIE CLK100M SSD N	12	30 67
TRUE	PCIE CLK100M SSD P	12	30 67
(Need to add 6 GND TPs)			

J4002: Camera Connector

FUNC_TEST			
TRUE	MIPI CLK CONN N	32	72
TRUE	MIPI CLK CONN P	32	72
TRUE	CAM SENSOR WAKE L CONN	32	
TRUE	MIPI DATA CONN N	32	72
TRUE	MIPI DATA CONN P	32	72
TRUE	SMBUS SMC 1 S0 SDA	14	32 37 40 43 44 69
TRUE	SMBUS SMC 1 S0 SCL	73	32 37 40 43 44 69
TRUE	I2C CAM SCK	31	32
TRUE	I2C CAM SDA	31	32
TRUE	PP5V S3RS0 ALSCAM F	32	
(Need to add 280 GND TPs)			

J6100: LPC+SPI Connector

FUNC_TEST			
TRUE	SPI ALT IO2 WP L	46	
TRUE	SPI ALT IO3 HOLD L	46	
TRUE	LPC AD<3..0>	14	37 69
TRUE	SPI ALT IO0 MOSI	46	
TRUE	XDP LPCPLUS GPIO	15	16
TRUE	LPCPLUS RESET L	59	
TRUE	SMC TDO	37	38
TRUE	TP SMC TRST L	37	38
TRUE	TP SMC MD1	37	38
TRUE	SMC TX L	37	38
TRUE	SPI ALT IO1 MISO	46	
TRUE	LPC FRAME L	14	37 69
TRUE	SPIROM USE MLB	15	46
TRUE	PM CLKRUN L	13	37
TRUE	SPI ALT CLK	46	
TRUE	SPI ALT CS L	46	
TRUE	LPC SERIRQ	15	37
TRUE	LPC PWRDWN L	13	37
TRUE	SMC TDI	37	38
TRUE	SMC TCK	37	38 46
TRUE	SMC RESET L	37	38 46 50
TRUE	SMC ROMBOOT	37	38
TRUE	SMC RX L	37	38
TRUE	SMC TMS	37	38 46
(Need to add 6 GND TPs)			

J4800: IPD Flex Connector

FUNC_TEST			
TRUE	SMC L1D	36	37 38 61 65
TRUE	TPAD SPI MISO R	36	
TRUE	USB TPAD P	14	36 68
TRUE	USB TPAD N	14	36 68
TRUE	TPAD SPI CLK R	36	
TRUE	TPAD WAKE L	36	
TRUE	TPAD SPI MOSI R	36	
TRUE	PP3V3 S4 IPD	36	
TRUE	TPAD SPI CS R L	36	
TRUE	TPAD SPI IP EN CONN	36	
TRUE	TPAD SPI INT S4 WAKE L CONN	36	
TRUE	PP5V S4 IPD	36	
TRUE	TPAD USB IP EN CONN	36	
TRUE	SMBUS SMC 3 SDA	36	37 40 44 73
TRUE	SMBUS SMC 3 SCL	36	37 40 44 73
TRUE	SMC LSOC RST L	36	38
TRUE	PP3V42 G3H	17	30 35 36 37 38 40 46 49 50
TRUE	SMC ONOFF L	36	37 38
(Need to add 5 GND TPs)			

J7000: DC-In Connector

FUNC_TEST		(Need 4 TPs)	
TRUE	PPDCIN G3H	49	50 62 64
TRUE	PP5V S4RS3	32	35 47 49 54 55 58 62
(Need to add 5 GND TPs)			

J6404: Speaker Connector

FUNC_TEST			
TRUE	SPKRAMP ROUT P	47	74
TRUE	SPKRAMP ROUT N	47	74
(Need to add 3 GND TPs)			

J6950: Battery Connector

FUNC_TEST		(Need 4 TPs)	
TRUE	PPVBAT G3H CONN	48	50
TRUE	SMBUS SMC 5 G3 SCL	37	40 48 50 73
TRUE	SMBUS SMC 5 G3 SDA	37	40 48 50 73
TRUE	SYS DETECT L	48	
(Need to add 4 GND TPs near J7050 and 1 for shield)			

J8300: Internal DP Connector

FUNC_TEST		(Need 2 TPs)	
TRUE	PPHV S0SW LCDBKLT	56	69 62
TRUE	LED RETURN 6	56	60
TRUE	LED RETURN 5	56	60
TRUE	LED RETURN 4	56	60
TRUE	LED RETURN 3	56	60
TRUE	LED RETURN 2	56	60
TRUE	LED RETURN 1	56	60
TRUE	DP INT HPD CONN	60	
TRUE	I2C TCON SDA R	60	
TRUE	I2C TCON SCL R	60	
TRUE	PP3V3 S0SW LCD UF	60	
TRUE	DP INT AUX CH C N	60	67
TRUE	DP INT AUX CH C P	60	67
TRUE	DP INT ML P<0>	60	67
TRUE	DP INT ML N<0>	60	67
(Need to add 5 GND TPs)			


J7715: KB BKLT Connector

FUNC_TEST			
TRUE	KBDLED ANODE	56	
TRUE	KBDLED FB	56	
(Need to add 2 GND TPs)			

J1800: XDP Connector

FUNC_TEST		(Only a subset are needed for PCT HW test fixture)	
TRUE	XDP CPU TCK	6	16 67
TRUE	XDP PCH TCK	12	16 69
TRUE	XDP CPU TDI	6	16 67
TRUE	XDP CPU TDO	6	16 67
TRUE	XDP CPUVCH TRST L	6	12 16 67
TRUE	XDP CPU TMS	6	16 67
TRUE	XDP PCH TMS	12	16 69
TRUE	XDP PCH TDI	12	16 69
TRUE	XDP PCH TDO	12	16 69
TRUE	XDP CPU FREQ L	6	16 67
TRUE	XDP CPU PRDY L	6	16 67
TRUE	XDP CPU VCCST PWRGD	16	
TRUE	PM RSMRST L	13	59
TRUE	XDP SYS PWROK	16	
TRUE	PM SYSRST L	13	37 37
TRUE	CPU CFG<3>	6	16 67
TRUE	PP1V05 S0	6	8 11 15 16 17 38 42 51 55 58
(Need to add 2 GND TPs)			

TRUE	PCH BT UART D2R	15
TRUE	PCH BT UART R2D	15
TRUE	PCH BT UART RTS L	15
TRUE	PCH BT UART CTS L	15
TRUE	AUD SPI CS L	15
TRUE	AUD SPI CLK	15
TRUE	AUD SPI MISO	15
TRUE	AUD SPI MOSI	15
TRUE	HDMITBTMUX LATCH	13
TRUE	HDD PWR EN	15
TRUE	WOL EN	14
TRUE	BT PWRST L	15
TRUE	HDMITBTMUX FLAG	13
TRUE	PW PWR EN	15
TRUE	FW PME L	15
TRUE	ENET MEDIA SENSE	15
TRUE	LCD PSR EN	15
TRUE	LCD IRQ L	15
TRUE	ODD PWR EN L	13
TRUE	ENET LOW PWR	13
TRUE	AUD IP PERIPHERAL DET	13
TRUE	AUD I2C INT L	13
TRUE	AP PCIE DEV WAKE	13

SYNC MASTER=WILL J43		SYNC DATE=12/17/2012			
PAGE TITLE					
Func Test / No Test					
 Apple Inc.		DRAWING NUMBER	SIZE		
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Functional Test Points

SD Card Aliases

J9500: LIO Connector

FUNC_TEST				MAKE_BASE				
TRUE	PP3V42_G3H	17	30 35 36 37 38 40 46 49 50	68 65 34 14	USB3_SD_D2R_P	TRUE	USB3_SD_D2R_P	14 34 65 68
TRUE	PP3V3_S0	62	64 74 89 81 82 84	68 65 34 14	USB3_SD_D2R_N	TRUE	USB3_SD_D2R_N	14 34 65 68
TRUE	PP1V5_S0SW_AUDIO	8	11 12 13 15 17 18 26 30 36 38	68 65 34 14	USB3_SD_R2D_C_P	TRUE	USB3_SD_R2D_C_P	14 34 65 68
TRUE	SYS_ONEWIRE	58	61	68 65 34 14	USB3_SD_R2D_C_N	TRUE	USB3_SD_R2D_C_N	14 34 65 68
TRUE	SMC_BC_ACOK	37	61					
TRUE	USB_PWR_EN	37	38 50 61	65 39 37 34 15	PP3V3_S0SW_SD		PP3V3_S0SW_SD	15 34 37 39 65
TRUE	SMBUS_SMC_2_S3_SDA	35	59 61					
TRUE	SMBUS_SMC_2_S3_SCL	37	40 61 73					
TRUE	SPKRAMP_SHDN_L	47	61					
TRUE	FINSTACKSNS_ALERT_L	39	61					
TRUE	SPKRAMP_INR_N	47	61 74					
TRUE	SPKRAMP_INR_P	47	61 74					
TRUE	USB_EXTB_N	14	61 68					
TRUE	USB_EXTB_P	14	61 68					
TRUE	PP5V_S0_ALT_AUD_LDO_EN	61						
TRUE	SMC_LID	36	37 38 61 64					
TRUE	HDA_SDOUT	12	61 69					
TRUE	HDA_BIT_CLK	12	61 69					
TRUE	HDA_SDIN0	12	61 69					
TRUE	XDP_USB_EXTB_OC_L	14	16 61					
TRUE	HDA_RST_L	12	61 69					
TRUE	HDA_SYNC	12	61 69					
TRUE	USB3_EXTB_D2R_RC_P	61	65 68					
TRUE	USB3_EXTB_D2R_RC_N	61	65 68					
TRUE	USB3_EXTB_R2D_P	61	65 68					
TRUE	USB3_EXTB_R2D_N	61	65 68					
TRUE	AUD_PWR_EN	13	59 61					

(MAKE_BASE=TRUE on page 45)

(Need to add 5 GND TPs)

Bead Probes

08 01 14	USB3_EXTB_D2R_N	TP	BEAD-PROBE	BPA511
08 01 14	USB3_EXTB_D2R_P	TP	BEAD-PROBE	BPA510
08 05 01	USB3_EXTB_D2R_RC_N	TP	BEAD-PROBE	BPA520
08 05 01	USB3_EXTB_D2R_RC_P	TP	BEAD-PROBE	BPA521
08 01 14	USB3_EXTB_R2D_C_N	TP	BEAD-PROBE	BPA513
08 01 14	USB3_EXTB_R2D_C_P	TP	BEAD-PROBE	BPA512
08 05 01	USB3_EXTB_R2D_N	TP	BEAD-PROBE	BPA523
08 05 01	USB3_EXTB_R2D_P	TP	BEAD-PROBE	BPA522

8		7		6		5		4		3		2		1	
J41/J43 Board-Specific Spacing & Physical Constraints															
BOARD LAYERS								BOARD AREAS				BOARD UNITS (MIL or MM)		ALLEGRO VERSION	
TOP, ISL2, ISL3, ISL4, ISL5, ISL6, ISL7, ISL8, ISL9, ISL10, ISL11, BOTTOM								NO_TYPE, BGA, MEM_TERM				MM		16.2	
PHYSICAL_RULE_SET	LAYER	ALLOW_ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP								
DEFAULT	TOP, BOTTOM	Y	=50_OHM_SE	=50_OHM_SE											
DEFAULT	ISL2, ISL11	Y	=45_OHM_SE	=45_OHM_SE											
DEFAULT	ISL3, ISL10	Y	=45_OHM_SE	=45_OHM_SE											
DEFAULT	ISL4, ISL9	Y	=45_OHM_SE	=45_OHM_SE											
DEFAULT	*	N	100 MM	100 MM	10 MM	0 MM	0 MM								
STANDARD	*	=DEFAULT	=DEFAULT	=DEFAULT	=DEFAULT	=DEFAULT	=DEFAULT								
Single-ended Physical Constraints															
PHYSICAL_RULE_SET	LAYER	ALLOW_ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP								
27P4_OHM_SE	TOP, BOTTOM	Y	0.310 MM	0.310 MM											
27P4_OHM_SE	ISL2, ISL11	Y	0.182 MM	0.182 MM											
27P4_OHM_SE	ISL3, ISL10	Y	0.182 MM	0.182 MM											
27P4_OHM_SE	ISL4, ISL9	Y	0.182 MM	0.182 MM											
27P4_OHM_SE	*	N	100 MM	100 MM	=STANDARD	=STANDARD	=STANDARD								
PHYSICAL_RULE_SET	LAYER	ALLOW_ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP								
35_OHM_SE	TOP, BOTTOM	Y	0.195 MM	0.195 MM											
35_OHM_SE	ISL2, ISL11	Y	0.125 MM	0.125 MM											
35_OHM_SE	ISL3, ISL10	Y	0.125 MM	0.125 MM											
35_OHM_SE	ISL4, ISL9	Y	0.125 MM	0.125 MM											
35_OHM_SE	*	N	100 MM	100 MM	=STANDARD	=STANDARD	=STANDARD								
PHYSICAL_RULE_SET	LAYER	ALLOW_ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP								
40_OHM_SE	TOP, BOTTOM	Y	0.170 MM	0.170 MM											
40_OHM_SE	ISL2, ISL11	Y	0.096 MM	0.096 MM											
40_OHM_SE	ISL3, ISL10	Y	0.096 MM	0.096 MM											
40_OHM_SE	ISL4, ISL9	Y	0.099 MM	0.099 MM											
40_OHM_SE	*	N	100 MM	100 MM	=STANDARD	=STANDARD	=STANDARD								
PHYSICAL_RULE_SET	LAYER	ALLOW_ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP								
45_OHM_SE	TOP, BOTTOM	Y	0.135 MM	0.135 MM											
45_OHM_SE	ISL2, ISL11	Y	0.075 MM	0.075 MM											
45_OHM_SE	ISL3, ISL10	Y	0.075 MM	0.075 MM											
45_OHM_SE	ISL4, ISL9	Y	0.080 MM	0.080 MM											
45_OHM_SE	*	N	100 MM	100 MM	=STANDARD	=STANDARD	=STANDARD								
PHYSICAL_RULE_SET	LAYER	ALLOW_ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP								
50_OHM_SE	TOP, BOTTOM	Y	0.110 MM	0.110 MM											
50_OHM_SE	*	N	100 MM	100 MM	=STANDARD	=STANDARD	=STANDARD								
PHYSICAL_RULE_SET	LAYER	ALLOW_ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP								
55_OHM_SE	TOP, BOTTOM	Y	0.090 MM	0.090 MM											
55_OHM_SE	*	N	100 MM	100 MM	=STANDARD	=STANDARD	=STANDARD								
Differential Pair Physical Constraints															
PHYSICAL_RULE_SET	LAYER	ALLOW_ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP								
70_OHM_DIFF	TOP, BOTTOM	Y	0.165 MM	0.165 MM		0.110 MM	0.110 MM								
70_OHM_DIFF	ISL2, ISL11	Y	0.105 MM	0.105 MM		0.100 MM	0.100 MM								
70_OHM_DIFF	ISL3, ISL10	Y	0.105 MM	0.105 MM		0.100 MM	0.100 MM								
70_OHM_DIFF	ISL4, ISL9	Y	0.110 MM	0.110MM		0.095 MM	0.095 MM								
70_OHM_DIFF	*	N	100 MM	100 MM	=STANDARD	=STANDARD	=STANDARD								
PHYSICAL_RULE_SET	LAYER	ALLOW_ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP								
80_OHM_DIFF	TOP, BOTTOM	Y	0.132 MM	0.132 MM		0.130 MM	0.130 MM								
80_OHM_DIFF	ISL2, ISL11	Y	0.081 MM	0.081 MM		0.115 MM	0.115 MM								
80_OHM_DIFF	ISL3, ISL10	Y	0.081 MM	0.081 MM		0.115 MM	0.115 MM								
80_OHM_DIFF	ISL4, ISL9	Y	0.088 MM	0.088 MM		0.110 MM	0.110 MM								
80_OHM_DIFF	*	N	100 MM	100 MM	=STANDARD	=STANDARD	=STANDARD								
PHYSICAL_RULE_SET	LAYER	ALLOW_ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP								
90_OHM_DIFF	TOP, BOTTOM	Y	0.115 MM	0.115 MM		0.200 MM	0.200 MM								
90_OHM_DIFF	ISL2, ISL11	Y	0.070 MM	0.070 MM		0.180 MM	0.180 MM								
90_OHM_DIFF	ISL3, ISL10	Y	0.070 MM	0.070 MM		0.180 MM	0.180 MM								
90_OHM_DIFF	ISL4, ISL9	Y	0.076 MM	0.076 MM		0.180 MM	0.180 MM								
90_OHM_DIFF	*	N	100 MM	100 MM	=STANDARD	=STANDARD	=STANDARD								
PHYSICAL_RULE_SET	LAYER	ALLOW_ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP								
73_OHM_DIFF	TOP, BOTTOM	Y	0.165 MM	0.165 MM		0.150 MM	0.150 MM								
73_OHM_DIFF	ISL2, ISL11	Y	0.106 MM	0.106 MM		0.150 MM	0.150 MM								
73_OHM_DIFF	ISL3, ISL10	Y	0.106 MM	0.106 MM		0.150 MM	0.150 MM								
73_OHM_DIFF	ISL4, ISL9	Y	0.110 MM	0.110 MM		0.150 MM	0.150 MM								
73_OHM_DIFF	*	N	100 MM	100 MM	=STANDARD	=STANDARD	=STANDARD								
PHYSICAL_RULE_SET	LAYER	ALLOW_ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP								
85_OHM_DIFF	TOP, BOTTOM	Y	0.120 MM	0.120 MM		0.150 MM	0.150 MM								
85_OHM_DIFF	ISL2, ISL11	Y	0.078 MM	0.078 MM		0.160 MM	0.160 MM								
85_OHM_DIFF	ISL3, ISL10	Y	0.078 MM	0.078 MM		0.160 MM	0.160 MM								
85_OHM_DIFF	ISL4, ISL9	Y	0.082 MM	0.082 MM		0.140 MM	0.140 MM								
85_OHM_DIFF	*	N	100 MM	100 MM	=STANDARD	=STANDARD	=STANDARD								
PHYSICAL_RULE_SET	LAYER	ALLOW_ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP								
90_OHM_DIFF	TOP, BOTTOM	Y	0.115 MM	0.115 MM		0.200 MM	0.200 MM								
90_OHM_DIFF	ISL2, ISL11	Y	0.070 MM	0.070 MM		0.180 MM	0.180 MM								
90_OHM_DIFF	ISL3, ISL10	Y	0.070 MM	0.070 MM		0.180 MM	0.180 MM								
90_OHM_DIFF	ISL4, ISL9	Y	0.076 MM	0.076 MM		0.180 MM	0.180 MM								
90_OHM_DIFF	*	N	100 MM	100 MM	=STANDARD	=STANDARD	=STANDARD								
PHYSICAL_RULE_SET	LAYER	ALLOW_ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP								
73_OHM_DIFF	TOP, BOTTOM	Y	0.165 MM	0.165 MM		0.150 MM	0.150 MM								
73_OHM_DIFF	ISL2, ISL11	Y	0.106 MM	0.106 MM		0.150 MM	0.150 MM								
73_OHM_DIFF	ISL3, ISL10	Y	0.106 MM	0.106 MM		0.150 MM	0.150 MM								
73_OHM_DIFF	ISL4, ISL9	Y	0.110 MM	0.110 MM		0.150 MM	0.150 MM								
73_OHM_DIFF	*	N	100 MM	100 MM	=STANDARD	=STANDARD	=STANDARD								
PHYSICAL_RULE_SET	LAYER	ALLOW_ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP								
85_OHM_DIFF	TOP, BOTTOM	Y	0.120 MM	0.120 MM		0.150 MM	0.150 MM								
85_OHM_DIFF	ISL2, ISL11	Y	0.078 MM	0.078 MM		0.160 MM	0.160 MM								
85_OHM_DIFF	ISL3, ISL10	Y	0.078 MM	0.078 MM		0.160 MM	0.160 MM								
85_OHM_DIFF	ISL4, ISL9	Y	0.082 MM	0.082 MM		0.140 MM	0.140 MM								
85_OHM_DIFF	*	N	100 MM	100 MM	=STANDARD	=STANDARD	=STANDARD								
PHYSICAL_RULE_SET	LAYER	ALLOW_ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP								
90_OHM_DIFF	TOP, BOTTOM	Y	0.115 MM	0.115 MM		0.200 MM	0.200 MM								
90_OHM_DIFF	ISL2, ISL11	Y	0.070 MM	0.070 MM		0.180 MM	0.180 MM								
90_OHM_DIFF	ISL3, ISL10	Y	0.070 MM	0.070 MM		0.180 MM	0.180 MM								
90_OHM_DIFF	ISL4, ISL9	Y	0.076 MM	0.076 MM		0.180 MM	0.180 MM								
90_OHM_DIFF	*	N	100 MM	100 MM	=STANDARD	=STANDARD	=STANDARD								
PHYSICAL_RULE_SET	LAYER	ALLOW_ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP								
73_OHM_DIFF	TOP, BOTTOM	Y	0.165 MM	0.165 MM		0.150 MM	0.150 MM								
73_OHM_DIFF	ISL2, ISL11	Y	0.106 MM	0.106 MM		0.150 MM	0.150 MM								
73_OHM_DIFF	ISL3, ISL10	Y	0.106 MM	0.106 MM		0.150 MM	0.150 MM								
73_OHM_DIFF	ISL4, ISL9	Y	0.110 MM	0.110 MM		0.150 MM	0.150 MM								
73_OHM_DIFF	*	N	100 MM	100 MM	=STANDARD	=STANDARD	=STANDARD								
PHYSICAL_RULE_SET	LAYER	ALLOW_ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP								
85_OHM_DIFF	TOP, BOTTOM	Y	0.120 MM	0.120 MM		0.150 MM	0.150 MM								
85_OHM_DIFF	ISL2, ISL11	Y	0.078 MM	0.078 MM		0.160 MM	0.160 MM								
85_OHM_DIFF	ISL3, ISL10	Y	0.078 MM	0.078 MM		0.160 MM	0.160 MM								
85_OHM_DIFF	ISL4, ISL9	Y	0.082 MM	0.082 MM		0.140 MM	0.140 MM								
85_OHM_DIFF	*	N	100 MM	100 MM	=STANDARD	=STANDARD	=STANDARD								
PHYSICAL_RULE_SET	LAYER	ALLOW_ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP								
90_OHM_DIFF	TOP, BOTTOM	Y	0.115 MM	0.115 MM		0.200 MM	0.200 MM								
90_OHM_DIFF	ISL2, ISL11	Y	0.070 MM	0.070 MM		0.180 MM	0.180 MM								
90_OHM_DIFF	ISL3, ISL10	Y	0.070 MM	0.070 MM		0.180 MM	0.180 MM								
90_OHM_DIFF	ISL4, ISL9	Y	0.076 MM	0.076 MM		0.180 MM	0.180 MM								
90_OHM_DIFF	*	N	100 MM	100 MM	=STANDARD	=STANDARD	=STANDARD								
PHYSICAL_RULE_SET	LAYER	ALLOW_ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP								
73_OHM_DIFF	TOP, BOTTOM	Y	0.165 MM	0.165 MM		0.150 MM	0.150 MM								
73_OHM_DIFF	ISL2, ISL11	Y	0.106 MM	0.106 MM		0.150 MM	0.150 MM								
73_OHM_DIFF	ISL3, ISL10	Y	0.106 MM	0.106 MM		0.150 MM	0.150 MM								
73_OHM_DIFF	ISL4, ISL9	Y	0.110 MM	0.110 MM		0.150 MM	0.150 MM								
73_OHM_DIFF	*	N	100 MM	100 MM	=STANDARD	=STANDARD	=STANDARD								
PHYSICAL_RULE_SET	LAYER	ALLOW_ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP								
85_OHM_DIFF	TOP, BOTTOM	Y	0.120 MM	0.120 MM		0.150 MM	0.150 MM								
85_OHM_DIFF	ISL2, ISL11	Y	0.078 MM	0.078 MM		0.160 MM	0.160 MM								
85_OHM_DIFF	ISL3, ISL10	Y	0.078 MM	0.078 MM		0.160 MM	0.160 MM								
85_OHM_DIFF	ISL4, ISL9	Y	0.082 MM	0.082 MM		0.140 MM	0.140 MM								
85_OHM_DIFF	*	N	100 MM	100 MM	=STANDARD	=STANDARD	=STANDARD								
PHYSICAL_RULE_SET	LAYER	ALLOW_ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP								
90_OHM_DIFF	TOP, BOTTOM	Y	0.115 MM	0.115 MM		0.200 MM	0.200 MM								
90_OHM_DIFF	ISL2, ISL11	Y	0.070 MM	0.070 MM		0.180 MM	0.180 MM								
90_OHM_DIFF	ISL3, ISL10	Y	0.070 MM	0.070 MM		0.180 MM	0.180 MM								
90_OHM_DIFF	ISL4, ISL9	Y	0.076 MM	0.076 MM		0.180 MM	0.180 MM								
90_OHM_DIFF	*	N	100 MM	100 MM	=STANDARD	=STANDARD	=STANDARD								
PHYSICAL_RULE_SET	LAYER	ALLOW_ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP								
73_OHM_DIFF	TOP, BOTTOM	Y	0.165 MM	0.165 MM		0.150 MM	0.150 MM								
73_OHM_DIFF	ISL2, ISL11	Y	0.106 MM	0.106 MM		0.150 MM	0.150 MM								
73_OHM_DIFF	ISL3, ISL10	Y	0.106 MM	0.106 MM		0.150 MM	0.150 MM								
73_OHM_DIFF	ISL4, ISL9	Y	0.110 MM	0.110 MM		0.150 MM	0.150 MM								
73_OHM_DIFF	*	N	100 MM	100 MM	=STANDARD	=STANDARD	=STANDARD								
PHYSICAL_RULE_SET	LAYER	ALLOW_ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP								
85_OHM_DIFF	TOP, BOTTOM	Y	0.120 MM	0.120 MM		0.150 MM	0.150 MM								
85_OHM_DIFF	ISL2, ISL11	Y	0.078 MM	0.078 MM		0.160 MM	0.160 MM								
85_OHM_DIFF	ISL3, ISL10	Y	0.078 MM	0.078 MM		0.160 MM	0.160 MM								
85_OHM_DIFF	ISL4, ISL9	Y	0.082 MM	0.082 MM		0.140 MM	0.140 MM								
85_OHM_DIFF	*	N	100 MM	100 MM	=STANDARD	=STANDARD	=STANDARD								
PHYSICAL_RULE_SET	LAYER	ALLOW_ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP								
90_OHM_DIFF	TOP, BOTTOM	Y	0.115 MM	0.115 MM		0.200 MM	0.200 MM								
90_OHM_DIFF	ISL2, ISL11	Y	0.070 MM	0.070 MM		0.180 MM	0.180 MM								
90_OHM_DIFF	ISL3, ISL10	Y	0.070 MM	0.070 MM		0.180 MM	0.180 MM								
90_OHM_DIFF	ISL4, ISL9	Y	0.076 MM	0.076 MM		0.180 MM	0.180 MM								
90_OHM_DIFF	*	N	100 MM	100 MM	=STANDARD	=STANDARD	=STANDARD								
PHYSICAL_RULE_SET	LAYER	ALLOW_ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP									

SATA Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SATA_80D	*	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA_ICOMP	*	=4x_DIELECTRIC	?

SOURCE: 471984_Chief_River_MS_PDG_1.0 and the spacing rule is adjusted per SI team feedback.

UART Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
UART_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
UART	*	=2x_DIELECTRIC	?

USB 2.0 Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCH_USB_BIAS	*	=STANDARD	8 MIL	8 MIL	=STANDARD	=STANDARD	=STANDARD
USB_8D	*	=0_OHM_DIFF	=0_OHM_DIFF	=0_OHM_DIFF	=0_OHM_DIFF	=0_OHM_DIFF	=0_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	*	=2x_DIELECTRIC	?

SOURCE: Calpella Platform Design Guide for Ibex Peak M (DG-398905-398905_v1.5), Section 3.8

USB 3.0 Interface Constraints

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET	SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB3_PCH_TX	USB3_PCH_TX	*	USB3_TX2TX	USB3_TX2TX	TOP,BOTTOM	=5x_DIELECTRIC	?
USB3_PCH_RX	USB3_PCH_RX	*	USB3_RX2RX	USB3_RX2RX	TOP,BOTTOM	=5x_DIELECTRIC	?
USB3_PCH_TX	*_PCH_TX	*	USB3_TX2OTHERTX	USB3_TX2OTHERTX	TOP,BOTTOM	=5x_DIELECTRIC	?
USB3_PCH_RX	*_PCH_RX	*	USB3_RX2OTHERRX	USB3_RX2OTHERRX	TOP,BOTTOM	=5x_DIELECTRIC	?
USB3_PCH_TX	*_PCH_RX	*	USB3_TX2RX	USB3_TX2RX	TOP,BOTTOM	=7x_DIELECTRIC	?
USB3_PCH_RX	*_PCH_TX	*	USB3_RX2TX	USB3_RX2TX	TOP,BOTTOM	=7x_DIELECTRIC	?
USB3_PCH_TX	*_TX	*	USB3_2OTHERHS	USB3_2OTHERHS	TOP,BOTTOM	=6x_DIELECTRIC	?
USB3_PCH_RX	*_TX	*	USB3_2OTHERHS	USB3_2OTHER	TOP,BOTTOM	=5x_DIELECTRIC	?
USB3_PCH_TX	*_RX	*	USB3_2OTHERHS				
USB3_PCH_RX	*_RX	*	USB3_2OTHERHS				
USB3_PCH_TX	*	*	USB3_2OTHER				
USB3_PCH_RX	*	*	USB3_2OTHER				

SOURCE: 471984_Cheif_River_MS_PDG_1.0 and the spacing rule is adjusted per SI team feedback.

PCH Net Properties


ELECTRICAL_CONSTRAINT_SET	NET_TYPE		
	PHYSICAL	SPACING	
PCH SATA_I0COMP		SATA_I0COMP	PCH SATAI0COMP
USB_HUB1_UP	USB_80D	USB	USB HUB UP P
USB_HUB1_UP	USB_80D	USB	USB HUB UP N
USB_BT	USB_80D	USB	USB BT P
USB_BT	USB_80D	USB	USB BT N
	USB_80D	USB	USB BT CONN P
	USB_80D	USB	USB BT CONN N
	USB_80D	USB	USB BT WAKE P
	USB_80D	USB	USB BT WAKE N
USB_TP4D	USB_80D	USB	USB TP4D P
USB_TP4D	USB_80D	USB	USB TP4D N
	USB_80D	USB	USB TP4D CONN P
	USB_80D	USB	USB TP4D CONN N
	USB_80D	USB	TP4D SPI MOSI USB P
	USB_80D	USB	TP4D SPI MISO USB N
USB_TP4D_M	USB_80D	USB	USB TP4D M P
USB_TP4D_M	USB_80D	USB	USB TP4D M N
USB_SDCARD	USB_80D	USB	USB SDCARD P
USB_SDCARD	USB_80D	USB	USB SDCARD N
	SET_45S	SP1	TP4D SPI MOSI
	SET_45S	SP2	TP4D SPI MISO
	SET_45S	SP2	TP4D SPI CLK
USB_EXT1	USB_80D	USB	USB EXT1 P
USB_EXT1	USB_80D	USB	USB EXT1 N
	UART_45S	UART	SMC DEBUGPRT TX L
	UART_45S	UART	SMC DEBUGPRT RX L
USB2_EXT1	USB_80D	USB	USB2_EXT1_MUXRD P
USB2_EXT1	USB_80D	USB	USB2_EXT1_MUXRD N
USB2_EXT1	USB_80D	USB	USB2_EXT1_MUXRD F P
USB2_EXT1	USB_80D	USB	USB2_EXT1_MUXRD F N
USB3_EXT1_RX	USB_80D	USB3_RCH_RX	USB3_EXT1_D2R P
USB3_EXT1_RX	USB_80D	USB3_RCH_RX	USB3_EXT1_D2R N
USB3_EXT1_TX	USB_80D	USB3_RCH_TX	USB3_EXT1_R2D P
USB3_EXT1_TX	USB_80D	USB3_RCH_TX	USB3_EXT1_R2D N
	USB_80D	USB3_RCH_RX	USB3_EXT1_D2R F P
	USB_80D	USB3_RCH_RX	USB3_EXT1_D2R F N
	USB_80D	USB3_RCH_TX	USB3_EXT1_R2D F P
	USB_80D	USB3_RCH_TX	USB3_EXT1_R2D F N
	USB_80D	USB3_RCH_TX	USB3_EXT1_R2D C P
	USB_80D	USB3_RCH_TX	USB3_EXT1_R2D C N
USB_EXTB	USB_80D	USB	USB_EXTB P
USB_EXTB	USB_80D	USB	USB_EXTB N
USB3_EXTB_RX	USB_80D	USB3_RCH_RX	USB3_EXTB_D2R P
USB3_EXTB_RX	USB_80D	USB3_RCH_RX	USB3_EXTB_D2R N
	USB_80D	USB3_RCH_RX	USB3_EXTB_D2R RC P
	USB_80D	USB3_RCH_RX	USB3_EXTB_D2R RC N
USB3_EXTB_TX	USB_80D	USB3_RCH_TX	USB3_EXTB_R2D P
USB3_EXTB_TX	USB_80D	USB3_RCH_TX	USB3_EXTB_R2D N
	USB_80D	USB3_RCH_TX	USB3_EXTB_R2D C P
	USB_80D	USB3_RCH_TX	USB3_EXTB_R2D C N
USB3_SD_RX	USB_80D	USB3_RCH_RX	USB3_SD_D2R P
USB3_SD_RX	USB_80D	USB3_RCH_RX	USB3_SD_D2R N
USB3_SD_TX	USB_80D	USB3_RCH_TX	USB3_SD_R2D C P
USB3_SD_TX	USB_80D	USB3_RCH_TX	USB3_SD_R2D C N
	USB_80D	USB3_RCH_RX	USB3_SD_D2R C P
	USB_80D	USB3_RCH_RX	USB3_SD_D2R C N
	USB_80D	USB3_RCH_TX	USB3_SD_R2D P
	USB_80D	USB3_RCH_TX	USB3_SD_R2D N
PCH_USB_DBTAS	PCH_USB_DBTAS		PCH_USB_RBIAS
PCH_DIPECLK_INUSED	CLK_PCIE_80D	CLK_PCIE	PCIE_CLK100M_PCH_P
PCH_DIPECLK_INUSED	CLK_PCIE_80D	CLK_PCIE	PCIE_CLK100M_PCH_N
PCH_DIPECLK_INUSED	CLK_PCIE_80D	CLK_PCIE	PCH_CLK96M_DOT_P
PCH_DIPECLK_INUSED	CLK_PCIE_80D	CLK_PCIE	PCH_CLK96M_DOT_N
PCH_DIPECLK_INUSED	CLK_PCIE_80D	CLK_PCIE	PCH_CLK100M_SATA_P
PCH_DIPECLK_INUSED	CLK_PCIE_80D	CLK_PCIE	PCH_CLK100M_SATA_N
PCH_DIPECLK_INUSED	CLK_45S	CLK_PCIE	PCH_CLK14P3M_REFCLK

USB Hucopyb nets

TP SPI nets

USB EXTA nets (Right USB port)

USB EXTB nets (Left USB port)

SYNC MASTER=CLEAN J43		SYNC DATE=11/13/2012	
PAGE TITLE			
PCH Constraints 1			
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Apple Inc.		REVISION <E4LABEL>	
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LPC Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
LPC_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
CLK_LPC_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
LPC	*	=3x_DIELECTRIC	?
CLK_LPC	*	=4x_DIELECTRIC	?

SOURCE: Calpella Platform Design Guide for Ibex Peak M (DG-398905-398905_v1.5), Section 3.15

SMBus Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SMB_45S_R_50S	TOP_BOTTOM	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE		
SMB_45S_R_50S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SMB	*	=2x_DIELECTRIC	?

HD Audio Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
HDA_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
HDA	*	=2x_DIELECTRIC	?

SOURCE: Calpella Platform Design Guide for Ixex Peak M (DG-398905-398905_v1.5), Section 3.15

SIO Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_SLOW_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_SLOW	*	= 4x_DIELECTRIC	?

SPI Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SP1_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SPI	*	=4x_DIELECTRIC	?

XDP Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCH_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCH_ITP	*	=2:1_SPACING	?

DisplayPort

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DP_80D	*	=0_OHM_DIFF	=0_OHM_DIFF	=0_OHM_DIFF	=0_OHM_DIFF	=0_OHM_DIFF	=0_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DP_2DP	*	=3x_DIELECTRIC	?
DP_2OTHERHS	*	=4x_DIELECTRIC	?
DP_2OTHER	*	=3x_DIELECTRIC	?
DP_AUX	*	=3x_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
DP_TX	DP_TX	*	DP_2DP
DP_TX	*_TX	*	DP_2OTHERHS
DP_TX	*_RX	*	DP_2OTHERHS
DP_TX	*	*	DP_2OTHER

System Clock Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_SLOW_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
CLK_25M_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
















SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_SLOW	*	=2x_DIELECTRIC	?
CLK_25M	*	=5x_DIELECTRIC	?

NOTE: 25MHz system clocks very sensitive to noise.

PCH Net Properties

ELECTRICAL_CONSTRAINT_SET		NET_TYPE		
		PHYSICAL	SPACING	
	LPC_AD	LPC_45S	LPC	LPC_AD<3..0>
	LPC_FRAME_L	LPC_45S	LPC	LPC_FRAME_L
		LPC_45S	LPC	LPCPLUS_RESET_L
	LPC_CLK32M	CLK LPC_45S	CLK LPC	LPC_CLK24M_SMC
		CLK LPC_45S	CLK LPC	LPC_CLK24M_SMC_R
	LPC_CLK32M	CLK LPC_45S	CLK LPC	LPC_CLK24M_LPCPLUS
		CLK LPC_45S	CLK LPC	LPC_CLK24M_LPCPLUS_R
	SMBUS_PCH_CLK	SMB_45S_R_50S	SMB	SMBUS_PCH_CLK
	SMBUS_PCH_DATA	SMB_45S_R_50S	SMB	SMBUS_PCH_DATA
	SMBUS_PCH_0_CLK	SMB_45S_R_50S	SMB	SMB_PCH_0_CLK
	SMBUS_PCH_0_DATA	SMB_45S_R_50S	SMB	SMB_PCH_0_DATA
	SMBUS_SMC_1_S0_SCL	SMB_45S_R_50S	SMB	SMBUS_SMC_1_S0_SCL
	SMBUS_SMC_1_S0_SDA	SMB_45S_R_50S	SMB	SMBUS_SMC_1_S0_SDA
	HDA_BIT_CLK	HDA_45S	HDA	HDA_BIT_CLK
		HDA_45S	HDA	HDA_BIT_CLK_R
	HDA_SYNC	HDA_45S	HDA	HDA_SYNC
		HDA_45S	HDA	HDA_SYNC_R
	HDA_RST_L	HDA_45S	HDA	HDA_RST_R_L
		HDA_45S	HDA	HDA_RST_L
	HDA_SDIO0	HDA_45S	HDA	HDA_SDIO0
	HDA_SDOUT	HDA_45S	HDA	HDA_SDOUT
		HDA_45S	HDA	HDA_SDOUT_R
	PM_SUS_CLK	CLK_SLOW_45S	CLK_SLOW	PM_CLK32K_SUSCLK_R
		CLK_SLOW_45S	CLK_SLOW	SMC_CLK32K
	SPI_CLK	SPI_45S	SPI	SPI_CLK_R
		SPI_45S	SPI	SPI_CLK
	SPI_MOSI	SPI_45S	SPI	SPI_MOSI_R
		SPI_45S	SPI	SPI_MOSI
	SPI_MISO	SPI_45S	SPI	SPI_MISO
		SPI_45S	SPI	SPI_MISO_R
	SPI_CS0	SPI_45S	SPI	SPI_CS0_R_L
		SPI_45S	SPI	SPI_CS0_L
		SPI_45S	SPI	SPI_SMC_CLK
		SPI_45S	SPI	SPI_SMC_MOSI
		SPI_45S	SPI	SPI_SMC_MISO
		SPI_45S	SPI	SPI_SMC_CS_L
		SPI_45S	SPI	SPI_MLB_CLK
		SPI_45S	SPI	SPI_MLB_IO0_MOSI
		SPI_45S	SPI	SPI_MLB_IO1_MISO
		SPI_45S	SPI	SPI_MLB_CS_L
		SPI_45S	SPI	SPI_IO<2>
		SPI_45S	SPI	SPI_IO2_R
		SPI_45S	SPI	SPI_MLB_IO2_WP_L
		SPI_45S	SPI	SPI_IO<3>
		SPI_45S	SPI	SPI_IO3_R
		SPI_45S	SPI	SPI_MLB_IO3_HOLD_L
	PCIE_AP_R2D	PCIE_80D	PCIE_PCH_TX	PCIE_AP_R2D_P
	PCIE_AP_R2D	PCIE_80D	PCIE_PCH_TX	PCIE_AP_R2D_N
		PCIE_80D	PCIE_PCH_TX	PCIE_AP_R2D_C_P
		PCIE_80D	PCIE_PCH_TX	PCIE_AP_R2D_C_N
	PCIE_AP_D2R	PCIE_80D	PCIE_PCH_RX	PCIE_AP_D2R_P
	PCIE_AP_D2R	PCIE_80D	PCIE_PCH_RX	PCIE_AP_D2R_N
	PCIE_CLK100M_AP	CLK PCIE_80D	CLK PCIE	PCIE_CLK100M_AP_P
	PCIE_CLK100M_AP	CLK PCIE_80D	CLK PCIE	PCIE_CLK100M_AP_N
	PCIE_TBT_R2D	PCIE_80D	PCIE_PCH_TX	PCIE_TBT_R2D_P<3..0>
	PCIE_TBT_R2D	PCIE_80D	PCIE_PCH_TX	PCIE_TBT_R2D_N<3..0>
		PCIE_80D	PCIE_PCH_TX	PCIE_TBT_R2D_C_P<3..0>
		PCIE_80D	PCIE_PCH_TX	PCIE_TBT_R2D_C_N<3..0>
	PCIE_TBT_D2R	PCIE_80D	PCIE_PCH_RX	PCIE_TBT_D2R_P<3..0>
	PCIE_TBT_D2R	PCIE_80D	PCIE_PCH_RX	PCIE_TBT_D2R_N<3..0>
		PCIE_80D	PCIE_PCH_RX	PCIE_TBT_D2R_C_P<3..0>
		PCIE_80D	PCIE_PCH_RX	PCIE_TBT_D2R_C_N<3..0>
	PCIE_CLK100M_TBT	CLK PCIE_80D	CLK PCIE	PCIE_CLK100M_TBT_P
	PCIE_CLK100M_TBT	CLK PCIE_80D	CLK PCIE	PCIE_CLK100M_TBT_N
		CLK PCIE_80D	CLK PCIE	PEG_CLK100M_P
		CLK PCIE_80D	CLK PCIE	PEG_CLK100M_N
	XDP_TDI	PCH_45S	PCH_TPE	XDP_PCH_TDI
	XDP_TDO	PCH_45S	PCH_TPE	XDP_PCH_TDO
	XDP_TMS	PCH_45S	PCH_TPE	XDP_PCH_TMS
	XDP_TCK	PCH_45S	PCH_TPE	XDP_PCH_TCK
	PCIE_CAMERA	PCIE_80D	PCIE_PCH_TX	PCIE_CAMERA_R2D_P
	PCIE_CAMERA	PCIE_80D	PCIE_PCH_TX	PCIE_CAMERA_R2D_N
		PCIE_80D	PCIE_PCH_TX	PCIE_CAMERA_R2D_C_P
		PCIE_80D	PCIE_PCH_TX	PCIE_CAMERA_R2D_C_N
	PCIE_CAMERA	PCIE_80D	PCIE_PCH_RX	PCIE_CAMERA_D2R_P
	PCIE_CAMERA	PCIE_80D	PCIE_PCH_RX	PCIE_CAMERA_D2R_N
		PCIE_80D	PCIE_PCH_RX	PCIE_CAMERA_D2R_C_P
		PCIE_80D	PCIE_PCH_RX	PCIE_CAMERA_D2R_C_N
	PCIE_CLK100M_CAMERA	CLK PCIE_80D	CLK PCIE	PCIE_CLK100M_CAMERA_P
	PCIE_CLK100M_CAMERA	CLK PCIE_80D	CLK PCIE	PCIE_CLK100M_CAMERA_N
		CLK PCIE_80D	CLK PCIE	PCIE_CLK100M_CAMERA_C_P
		CLK PCIE_80D	CLK PCIE	PCIE_CLK100M_CAMERA_C_N

Clock Net Properties

ELECTRICAL_CONSTRAINT_SET		NET_TYPE		
		PHYSICAL	SPACING	
	SYSCLK CLK32K RTC	CLK 32M 45S	CLK 32M	SYSCLK CLK32K RTCX1
	SYSCLK CLK25M SB	CLK 25M 45S	CLK 25M	SYSCLK CLK25M CAMERA
		CLK 25M 45S	CLK 25M	CLK25M CAM CLKP
		CLK 25M 45S	CLK 25M	CLK25M CAM XTALP R
		CLK 25M 45S	CLK 25M	CLK25M CAM XTALP
		CLK 25M 45S	CLK 25M	CLK25M CAM XTALN
		CLK 25M 45S	CLK 25M	CLK25M CAM CLKKN
	SYSCLK CLK25M TBT	CLK 25M 45S	CLK 25M	SYSCLK CLK25M TBT
		CLK 25M 45S	CLK 25M	SYSCLK CLK25M TBT R
	SYSCLK CLK25M XTAL	CLK 25M 45S	CLK 25M	SYSCLK CLK25M X1
		CLK 25M 45S	CLK 25M	SYSCLK CLK25M X2
		CLK 25M 45S	CLK 25M	SYSCLK CLK25M X2 R
		CLK 25M 45S	CLK 25M	SDCLK CLK25M X2
		CLK 25M 45S	CLK 25M	SDCLK CLK25M X2 R
		CLK 25M 45S	CLK 25M	SDSClk CLK25M X1

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MIPI Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW_ROUTE_ON_LAYER?	MINIMUM_LINE_WIDTH	MINIMUM_NECK_WIDTH	MAXIMUM_NECK_LENGTH	DIFFPAIR_PRIMARY_GAP	DIFFPAIR_NECK_GAP
MIPI_85D	*	=45_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE_SPACING	WEIGHT	SPACING_RULE_SET	LAYER	LINE-TO-LINE_SPACING	WEIGHT
MIPI_20THER	*	=4x_DIELECTRIC	?	MIPI_20THER	TOP,BOTTOM	=4x_DIELECTRIC	?
MIPI_SCLK	*	=4x_DIELECTRIC	?	MIPI_SCLK	TOP,BOTTOM	=4x_DIELECTRIC	?
MIPICLK_20THER	*	=7x_DIELECTRIC	?	MIPICLK_20THER	TOP,BOTTOM	=10x_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MIPI_DATA	*	*	MIPI_20THER
MIPI_DATA	CLK_MIPI	*	MIPI_2CLK
CLK_MIPI	*	*	MIPICLK_20THER

Memory Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW_ROUTE_ON_LAYER?	MINIMUM_LINE_WIDTH	MINIMUM_NECK_WIDTH	MAXIMUM_NECK_LENGTH	DIFFPAIR_PRIMARY_GAP	DIFFPAIR_NECK_GAP
S2_MEM_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
S2_MEM_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

Spacing Rule Sets

SPACING_RULE_SET	LAYER	LINE-TO-LINE_SPACING	WEIGHT	SPACING_RULE_SET	LAYER	LINE-TO-LINE_SPACING	WEIGHT
S2_DATA2SELF	*	=2x_DIELECTRIC	?	S2_DATA2SELF	TOP,BOTTOM	=4x_DIELECTRIC	?
S2_DQS20WNDATA	*	=2x_DIELECTRIC	?	S2_DQS20WNDATA	TOP,BOTTOM	=4x_DIELECTRIC	?
S2_CMD2CMD	*	=2x_DIELECTRIC	?	S2_CMD2CMD	TOP,BOTTOM	=4x_DIELECTRIC	?
S2_CMD2CTRL	*	=2x_DIELECTRIC	?	S2_CMD2CTRL	TOP,BOTTOM	=4x_DIELECTRIC	?
S2_CTRL2CTRL	*	=2x_DIELECTRIC	?	S2_CTRL2CTRL	TOP,BOTTOM	=4x_DIELECTRIC	?
S2_20THERMEM	*	=4x_DIELECTRIC	?	S2_20THERMEM	TOP,BOTTOM	=6x_DIELECTRIC	?
S2MEM_2PWR	*	=2x_DIELECTRIC	?	S2MEM_2PWR	TOP,BOTTOM	=4x_DIELECTRIC	?
S2MEM_2GND	*	=2x_DIELECTRIC	?	S2MEM_2GND	TOP,BOTTOM	=4x_DIELECTRIC	?
S2MEM_2OTHER	*	=6x_DIELECTRIC	?	S2MEM_2OTHER	TOP,BOTTOM	=10x_DIELECTRIC	?

Memory Bus Spacing Group Assignments

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
S2_MEM_DATA*	*	*	S2MEM_20THER
S2_MEM_DQS*	*	*	S2MEM_20THER
S2_MEM_CMD	*	*	S2MEM_20THER
S2_MEM_CTRL	*	*	S2MEM_20THER
S2_MEM_CLK	*	*	S2MEM_20THER
S2_MEM_DATA*	=SAME	*	S2_DATA2SELF
S2_MEM_CMD	S2_MEM_CMD	*	S2_CMD2CMD
S2_MEM_CMD	S2_MEM_CTRL	*	S2_CMD2CTRL
S2_MEM_CTRL	S2_MEM_CTRL	*	S2_CTRL2CTRL
S2_MEM_*	S2_MEM_*	*	S2_20THERMEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
S2_MEM_DQS1	S2_MEM_DATA1	*	S2_DQS20WNDATA
S2_MEM_DQS0	S2_MEM_DATA0	*	S2_DQS20WNDATA

Memory to Power Spacing

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
S2_MEM_PWR	S2_MEM_*	*	S2MEM_2PWR
S2_MEM_PWR	*	*	DEFAULT

Memory to GND Spacing

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
GND	S2_MEM_*	*	S2MEM_2GND

Camera Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE			
	PHYSICAL	SPACING		
S2_MEM_CLK	S2_MEM_85D	S2_MEM_CLK	MEM_CAM_CLK_P	31 32
S2_MEM_CLK	S2_MEM_85D	S2_MEM_CLK	MEM_CAM_CLK_N	31 32
S2_MEM_CTRL	S2_MEM_45S	S2_MEM_CTRL	MEM_CAM_CKE	31 32
S2_MEM_CTRL	S2_MEM_45S	S2_MEM_CTRL	MEM_CAM_CS_L	31 32
S2_MEM_CMD	S2_MEM_45S	S2_MEM_CTRL	MEM_CAM_ODT	32
S2_MEM_CMD	S2_MEM_45S	S2_MEM_CTRL	MEM_CAM_CAS_L	31 32
S2_MEM_CMD	S2_MEM_45S	S2_MEM_CTRL	MEM_CAM_RAS_L	31 32
S2_MEM_CMD	S2_MEM_45S	S2_MEM_CMD	MEM_CAM_WE_L	31 32
S2_MEM_CMD	S2_MEM_45S	S2_MEM_CMD	MEM_CAM_BA<0>	31 32
S2_MEM_CMD	S2_MEM_45S	S2_MEM_CMD	MEM_CAM_BA<1>	31 32
S2_MEM_CMD	S2_MEM_45S	S2_MEM_CMD	MEM_CAM_BA<2>	31 32
S2_MEM_DQS0	S2_MEM_85D	S2_MEM_DQS0	MEM_CAM_DQS_P<0>	31 32
S2_MEM_DQS0	S2_MEM_85D	S2_MEM_DQS0	MEM_CAM_DQS_N<0>	31 32
S2_MEM_DQS1	S2_MEM_85D	S2_MEM_DQS1	MEM_CAM_DQS_P<1>	31 32
S2_MEM_DQS1	S2_MEM_85D	S2_MEM_DQS1	MEM_CAM_DQS_N<1>	31 32
S2_MEM_DATA_0	S2_MEM_45S	S2_MEM_DATA0	MEM_CAM_DM<0>	31 32
S2_MEM_DATA_1	S2_MEM_45S	S2_MEM_DATA1	MEM_CAM_DM<1>	31 32
S2_MEM_A	S2_MEM_45S	S2_MEM_CMD	MEM_CAM_A<14..0>	31 32
S2_MEM_DATA_0	S2_MEM_45S	S2_MEM_DATA0	MEM_CAM_DQ<7..0>	31 32
S2_MEM_DATA_1	S2_MEM_45S	S2_MEM_DATA1	MEM_CAM_DQ<15..8>	31 32
MIPI_DATA_S2	MIPI_85D	MIPI_DATA	MIPI_DATA_P	31 32
MIPI_DATA_S2	MIPI_85D	MIPI_DATA	MIPI_DATA_N	31 32
MIPI_DATA_S2	MIPI_85D	MIPI_DATA	MIPI_DATA_CONN_P	32 64
MIPI_DATA_S2	MIPI_85D	MIPI_DATA	MIPI_DATA_CONN_N	32 64
MIPI_CLK_S2	MIPI_85D	CLK_MIPI	MIPI_CLK_P	31 32
MIPI_CLK_S2	MIPI_85D	CLK_MIPI	MIPI_CLK_N	31 32
MIPI_CLK_S2	MIPI_85D	CLK_MIPI	MIPI_CLK_CONN_P	32 64
MIPI_CLK_S2	MIPI_85D	CLK_MIPI	MIPI_CLK_CONN_N	32 64
		S2_MEM_PWB	PP1V35_CAM	31 32
		S2_MEM_PWB	PP0V675_CAM_VREF	31 32
		S2_MEM_PWB	PP0V675_MEM_CAM_VREFCA	32
		S2_MEM_PWB	PP0V675_MEM_CAM_VREFDQ	32

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Camera Constraints			
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